Trends in Development of Epitaxial Wafers for Emerging Devices Applied to Ultra-low Power-Consumption Integrated Circuits

Sumitomo Chemical Co., Ltd.
IT-related Chemicals Research Laboratory
Masafumi YOKOYAMA
Taketsugu YAMAMOTO

With recent dramatic increases in information, power consumption is an important issue for data processes, and ultra-low power switching devices are required. The emerging transistors with lower power consumption operation are required instead of the conventional ones. Tunnel field-effect transistors have attracted much attention as ultra-low power operating devices. We report the recent progress in tunnel field-effect transistors based on the III-V compound semiconductors and in the III-V epitaxial wafers for next generation devices.

This paper is translated from R&D Report, "SUMITOMO KAGAKU", vol. 2017.

Tunnel Transistors as Ultra-low Power Consuming Devices

As is symbolized by data storage centers, information systems have increased in speed and in capacity in recent years. The power consumption by information processing tends to increase with this trend. In addition, the use of mobile devices has spread explosively, and the era of the Internet of Things (IoT) in which all things are connected to the Internet has been reached. The necessity for reduction of the power consumption in information processing is tending to increase. With this background, processors that can operate with low power consumption are needed in the world.

Conventionally, metal-oxide-semiconductor field-effect transistors (MOSFETs), which have silicon (Si) as a channel material, have been used in processors. Since the power consumed by transistors is proportional to the square of the supply voltage (V_{DD}), reducing the supply voltage is effective for reducing power consumption. Miniaturization of devices can reduce the supply voltage for Si MOSFETs.[1] In addition, the use of channel materials with high electron (or hole) mobility instead of Si has been investigated.[2)–4)]

Up to now increases in the processing speed and reductions in power consumption for devices have been achieved by miniaturization of the devices. Currently, miniaturization has reached approximately 10 nm, and the limitations of miniaturization in two-dimensional scaling will be approached. It is predicted that the demise of miniaturization in two-dimensional structures will come by 2024.[1]

On the other hand, the high mobility materials such as III-V compound semiconductors and geranium (Ge) for channel materials instead of Si have been studied for low power consumption devices.[2)–4)] However, the S factor, which is the reciprocal of the steepness of the rise of current-voltage characteristics, has a limit of 60 mV/decade at room temperature in terms of operating principles for MOSFETs. Therefore, even if high mobility materials are used for channels, the supply voltage will be limited to approximately 0.5 V. For further reduction of power consumption by reduction of the supply voltage, it is desirable to be able to achieve S factors of smaller than 60 mV/decade by an operating principle different from conventional MOSFETs, leading to transistors that can operate at lower supply voltages.

Thus, tunnel field-effect transistors (TFETs) have attracted attention as new low power consumption devices.[5)–9)] Sumitomo Chemical Co., Ltd. has also participated in the JST Strategic Basic Research Program for "Creation of Revolutionary Nano Electronics Fusing Materials, Devices and Systems: Construction of Tunnel MOSFET Technology for Ultra-low Power Consumption Integrated Circuits" (abbreviated TFET-PJ in the following) since 2013 and has been developing TFETs. In this paper, we review the results of this project and the trends in related technologies.

1. Reduced Power Consumption Using TFETs

TFETs can achieve S factors of sub-60 mV/decade by controlling tunnel current using the field effect between the source and channel junction, and it is possible to reach a V_{DD} of 0.5 V or less. Thus, there are expectations for their development as new devices that can achieve steeper current rise characteristics than conventional MOSFETs.[1),5)–9)] **Fig. 1** shows a schematic illustration of the current-voltage characteristics (*I-V* characteristics) of TFETs and MOSFETs. Since the V_{DD} for obtaining the same ON current (I_{ON}) is reduced if the S factor is smaller, that is the slope is steeper, it is possible to reduce energy consumption. Furthermore, if the slope is steeper, the OFF current (I_{OFF}) tends to decrease, and it can be expected that power consumption during standby will be suppressed.

Fig. 2 shows a schematic illustration of an n-type TFET and operating principles. Here, E_G is the bandgap,

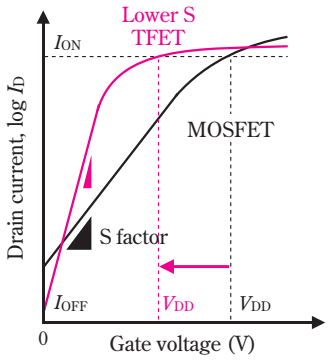

Fig. 1 Schematic illustration of *I-V* characteristics of a TFET and a MOSFET. A TFET can achieve lower S factor than a MOSFET.

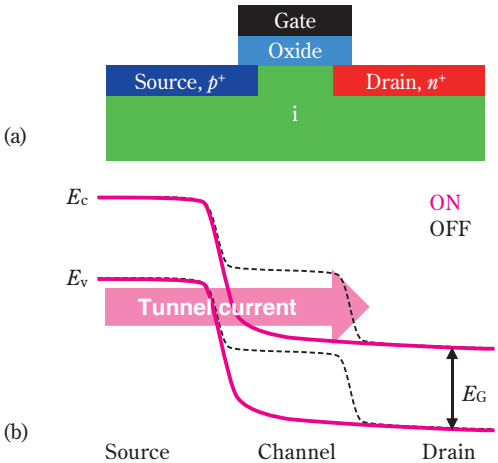

Fig. 2 Schematic illustration of (a) structure and (b) principle of operation of an n-type TFET

E_C is the energy at the bottom of the conduction band, and E_V is the energy at the top of the valence band. The operation of the TFETs is based on band-to-band tunneling (BTBT) of electrons. A p^+ region is formed as the source region and an n^+ region is formed as the drain region, respectively. The tunnel current from the source to the channel is controlled by the gate field effect. In the OFF state, the tunnel barrier is high, and the tunnel current is suppressed. On the contrary, in the ON state, the tunnel barrier is made low by the gate field effect, and the tunnel current flows. A lower S factor can be achieved in *I-V* characteristics compared to the conventional MOSFETs.

On the other hand, a TFET can suffer from a low drive current because of the tunnel resistance. In order to enhance the drive current of the TFET, narrow bandgap materials with a lower tunnel resistance than Si have been studied to achieve a high drive current for TFET channel material.[5)–13)] **Fig. 3** shows the tunneling current density (J) in typical semiconductor materials as a function of the electric fields calculated by using Equation (1), where m_r^* is the tunneling effective mass, q is the elementary electric charge, ξ is the electric field strength, V_R is the reverse bias voltage, and $\hbar = h/2\pi$, where h is Planck's constant, respectively. Here, the maximum electric field is assumed to be sufficiently high. **Table 1** shows the bandgap and m_r^* in semiconductors,[14)] where m_r^* is given by $m_r^* = m_e^* m_h^* / (m_e^* + m_h^*)$, and m_e^* is the effective mass of electrons, m_h^* is the effective mass of holes, and m_0 is the electron mass,

$$J = \frac{\sqrt{2m_r^*}\, q^3 \xi V_R}{8\pi^2 \hbar^2 E_G^{1/2}} \exp\left(-\frac{4\sqrt{2m_r^*}\, E_G^{3/2}}{3q\xi\hbar}\right) \quad (1)$$

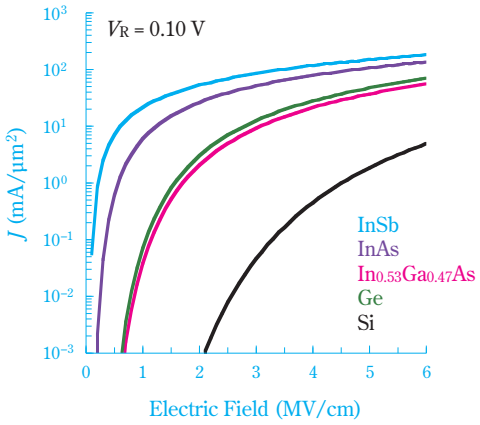

Fig. 3 Calculated tunneling current density versus electric field properties of semiconductors at a V_R of 0.10 V at 300 K

Table 1 Material physical parameters of energy band gap and tunneling effective mass of semiconductors

Semiconductors	E_G (eV)	m_r^*
InSb	0.17	0.007 m_0
InAs	0.35	0.012 m_0
$In_{0.53}Ga_{0.47}As$	0.74	0.023 m_0
Ge	0.66	0.028 m_0
Si	1.12	0.087 m_0

respectively. As shown in **Fig. 3**, III-V compound semiconductors with a narrow bandgap, such as InSb, InAs and $In_{0.53}Ga_{0.47}As$, show a high tunneling current density, indicating that they can allow us to realize a high driven current for TFETs.

TFET Using III-V Compound Semiconductors for Channel Material

1. Development of InGaAs TFET

III-V compound semiconductors with a narrow bandgap have been investigated in order to achieve a high performance TFET with both a good S factor and high ON current.[8),9),11)–13)] Among the III-V compound semiconductors, InGaAs is a row bandgap material with a bandgap of approximately 0.74 eV at room temperature, when an In content is 0.53. In addition, since InGaAs with an In content of 0.53 can be lattice matched to InP, an epitaxial layer with high crystal quality can be grown on an InP (100) substrate.

Fig. 4 shows a schematic illustration of an InGaAs TFET fabricated on an InP (100) substrate. The fabrication processes of the TFET are as follows. First, an InGaAs layer is grown on an InP (100) substrate using a metal-organic chemical vapor deposition (MOCVD). Here, a commercial production furnace is used for the fabrication of the epitaxial substrate. Subsequently, the source region, gate oxide, gate electrode, and drain region are formed on the InGaAs layer, and the InGaAs TFET is completed.

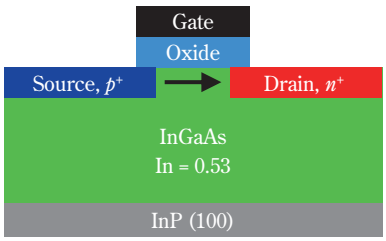

Fig. 4 Schematic illustration of the InGaAs TFET with $In_{0.53}Ga_{0.47}As$ channel grown on InP (100) substrate. A source region can be formed by Zn diffusion and a drain region can be formed by Ni-InGaAs alloy formation.
Figure created by using data provided by collaborators (Ref. 11)

The source region of the TFET is generally formed by doping, and a high doping concentration in the source region and a steepness in the impurity profile of the source junction are important for achieving a small S factor. In the TFET-PJ, doping in TFETs in which the channel layer is InGaAs was performed by a spin-on-glass (SOG) method for zinc (Zn), which is a p-type dopant for InGaAs, to form the source region.[11),12)] A Zn doping concentration of 2×10^{19} atoms/cm^3 was achieved by optimizing annealing treatment conditions. In addition, the diffusion coefficient of Zn in InGaAs is proportional to the square of the Zn doping concentration, and a steepness in the Zn impurity profile of 3.5 nm/decade can be achieved.[11),12)] The fabrication processes of InGaAs TFETs were as follows. After the source region was formed by the Zn diffusion process, the gate oxide film and gate electrode were formed. Subsequently, the drain region was formed by Ni-InGaAs using Ni-InGaAs alloy formation processes.[15)]

Fig. 5 shows the device characteristics of an InGaAs TFET with the In content of 0.53 in which the source region was formed by the Zn solid phase diffusion using Zn doped SOG. Here, the drain current (I_D) is shown in **Fig. 5** as a function of the gate voltage (V_G) with a drain voltage (V_D) of 0.15 V. The InGaAs TFET shows the S factor of 64 mV/decade and an ON current/OFF

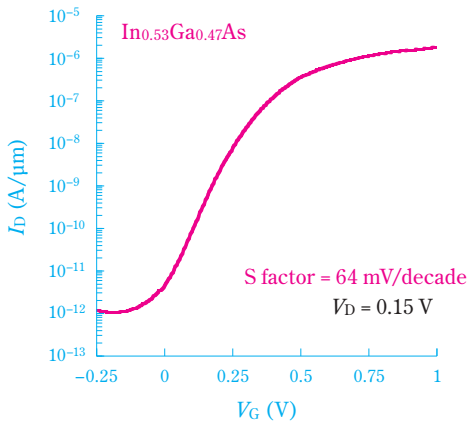

Fig. 5 Measured I_D-V_G characteristic of an $In_{0.53}Ga_{0.47}As$ TFET with the source region formed by Zn diffusion at 500 °C
Figure created by using data provided by collaborators (Ref. 11)

current ratio exceeding 10^6 at room temperature. The good characteristics of the OFF current indicate that the source junction formation processes by the Zn diffusion using Zn doped SOG can suppress the generation of crystal defects during the source junction formation processes. It is possible to make use of the excellent crystallinity of the epitaxially grown InGaAs channel layer because the source and drain regions can be formed with suppression of the generation of defects.

The source region formation by the Zn solid phase diffusion was also followed by another organization.[16] In addition, it was reported that the source region formation by the Zn gas phase diffusion can achieve a Zn impurity doping profile with a steepness of 4.7 nm/decade and a Zn doping concentration of 2×10^{19} atoms/cm^3 in the direction of depth.[17]

2. Investigation of High In content InGaAs Channel Layer for InGaAs TFET

The bandgap of InGaAs can be narrow with the increase in the In content, resulting in enhancement of the tunnel current. Therefore, it can be expected that high ON current can be achieved in InGaAs TFETs by making the In content in the InGaAs layer higher than 0.53. **Fig. 6** shows calculated results of the tunneling current density of the InGaAs with In contents of 0.53, 0.60, 0.65, 0.70, 0.80, 0.90, and 1.00 as a function of the electric field. The tunneling current density is increased by increasing the In content. However, it is difficult to grow an InGaAs channel with a high In content on an InP substrate because of the lattice mismatching between the InP substrate and the InGaAs layer. When an InGaAs layer with an In content of 0.53 which is lattice matched to InP is epitaxially grown on an InP substrate, it can maintain high level crystallinity even with a sufficiently thick film growth. On the other hand, when there is a difference in lattice constant between the substrate and the grown layer, the film thickness which can be grown without lattice relaxation is limited.[18)–21)] In epitaxial growth of an InGaAs layer on an InP substrate, the lattice mismatch to the InP substrate increases with the increase in the In content. Therefore, the critical thickness of an InGaAs layer can be limited with the increase in the In content. The crystal defects generated by lattice relaxation can be a cause of a leakage current. **Fig. 7** shows the device characteristics for InGaAs TFETs fabricated using substrates in which an InGaAs layer with In content of 0.53 and 0.70 were grown on an InP (100) substrate.[12] Here, the thickness of the InGaAs layer is 100 nm. It was found that the ON current increased by increasing the In content of the InGaAs layer. On the other hand, it was found that the OFF current and S factor are also increased by increasing the In content of the InGaAs layer. These results

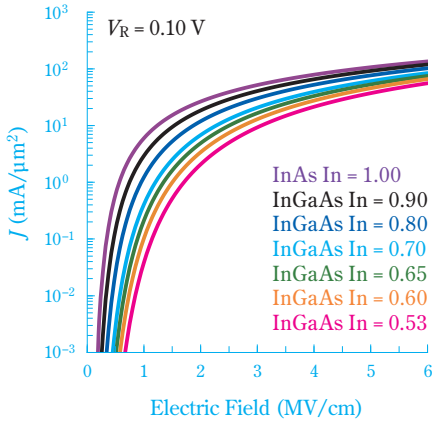

Fig. 6 Calculated tunneling current density versus electric field properties of $In_xGa_{1-x}As$ with In content of 0.53 – 1.00 at a V_R of 0.10 V at 300 K

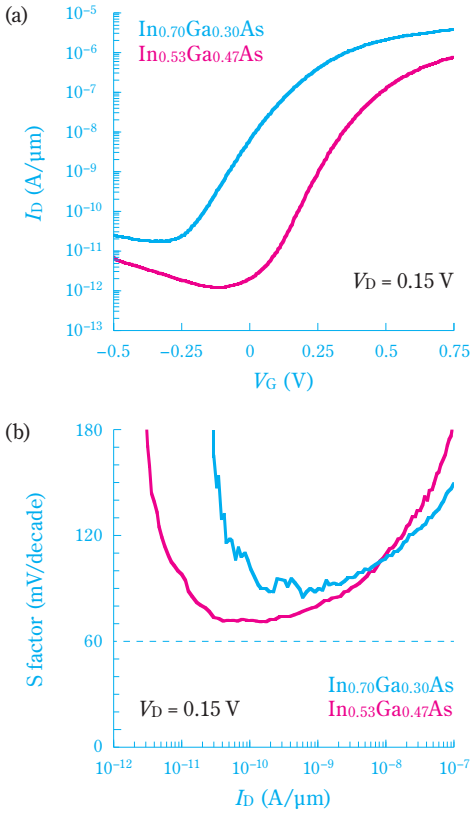

Fig. 7 (a) Measured I_D-V_G characteristics and (b) measured S factor as a function of I_D for InGaAs TFETs with In content of 0.53 and 0.70. Here, the thickness of InGaAs is 100 nm.
Figure created by using data provided by collaborators (Ref. 12)

indicate that the defects caused by the lattice mismatch between the high In content InGaAs and InP can affect the device performance. Therefore, it is important to suppress crystal defects when growing InGaAs layers with a high In content.

3. Investigation of High In Content InGaAs Quantum Wells for TFETs

It is important for TFETs to achieve a low OFF current at the same time as well as a high ON current. Because standby energy consumption can be suppressed, the suppression of the OFF current is important in low power consumption devices. Therefore, a leakage current caused by defects must be suppressed in InGaAs TFETs with high In content InGaAs layers, and the crystallinity of the channel layer must be improved. In the TFET-PJ, InGaAs TFETs with a quantum well (QW) channel have been developed with a high In content InGaAs channel layer. High In content InGaAs QW channel layers are set to be 10 nm or less in order to maintain the crystallinity of the high In content InGaAs channel layers and suppress crystal defects caused by lattice relaxation.[8),13)] Electrical controllability can be increased by confinement of carriers in the QW channel layer. **Fig. 8** shows a schematic diagram of an InGaAs QW TFET having an InGaAs QW channel with a high In content. The structure is one in which the high In content layer is sandwiched between InGaAs layers with an In content of 0.53. Thus, formation of the InGaAs channel layer with a high In content having good crystallinity can be expected. In addition, the junction with the substrate side in the source region is a junction with InGaAs with an In content of 0.53, and it is expected that the junction leakage current can be suppressed. **Fig. 9** shows the *I-V* characteristics for an InGaAs QW TFET having an InGaAs QW channel with an In content of 0.70 and with a QW layer thickness of 3 nm. For comparison, the *I-V* characteristics of an InGaAs bulk TFET with a single layer InGaAs having an In of 0.53 is shown. The source current (I_S) versus V_G curves with V_D of 0.15 V are shown in **Fig. 9**. As with the increase in ON current compared with the InGaAs TFET with an In content of 0.53, the minimum value for the OFF current could be reduced by a factor of 10 or more compared with the InGaAs TFET with the In content of 0.70 and a film thickness of 100 nm shown in **Fig. 7** (a) by the use of the high In content InGaAs QW channel structure. An S factor of 62 mV/decade was achieved. Thus, TFET device characteristics could be improved by forming the channel layer using advanced epitaxial growth technologies.

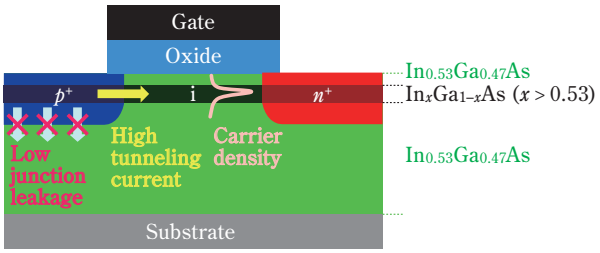

Fig. 8 Schematic illustration of the $In_xGa_{1-x}As$ QW TFET with high In content $In_xGa_{1-x}As$ QW structure
Figure created by using data provided by collaborators (Ref. 13)

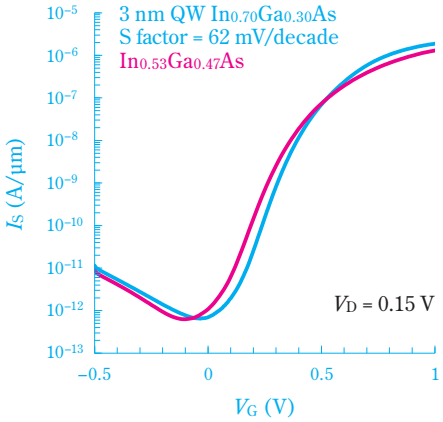

Fig. 9 I_S-V_G characteristics of a 3-nm-thick $In_{0.70}Ga_{0.30}As$ QW TFET and a control bulk $In_{0.53}Ga_{0.47}As$ TFET
Figure created by using data provided by collaborators (Ref. 13)

4. Improvement of TFET by Scaling of Gate Oxide Film

Scaling of gate oxide film, making the oxide films thinner, can be effective for improving OFF characteristics and S factors of TFET.[8),9),11)–13),17)] **Fig. 10** shows the impact of the gate oxide film scaling in an InGaAs TFET with an In content of 0.53. Here, the gate oxide film thickness is shown by capacitance equivalent thickness (CET). In the TFET-PJ, improvements in the S factor were confirmed with CET scaling. An S factor of 57 mV/decade at room temperature was achieved by scaling CET to 1.7 nm in an InGaAs TFET with an In content of 0.53.[13)] Furthermore, an S factor of 55 mV/decade at room temperature was achieved by using film thinning on the gate oxide film in an InGaAs QW TFET with a high In content.[8)]

It is very important that high performance TFETs

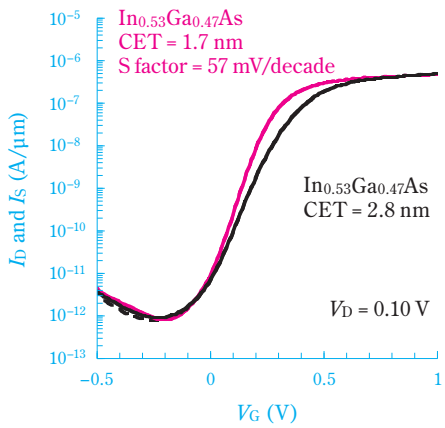

Fig. 10 I_D-V_G (solid) and I_S-V_G (broken) curves of bulk $In_{0.53}Ga_{0.47}As$ TFETs with CET of 1.7 and 2.8 nm
Figure created by using data provided by collaborators (Ref. 13)

have been achieved by using high quality epitaxial wafers fabricated by a commercial production MOCVD in the TFET-PJ. Further improvement of TFET performance can be achieved by the synergy of crystal growth and device processes.

5. Heterojunction based TFET

In order to achieve high level device performance of TFETs, it has been attractive to use heterojunctions for source and channel junctions.[5)–9),22)–32)] Heterojunctions can make the effective bandgap narrow by controlling the band alignment of different materials. As a result, high ON currents can be expected to be achieved. **Fig. 11** shows a schematic diagram of a heterojunction based TFET. The effective bandgap (ΔE_G) can be controlled by combining different materials. Here, E_{G_1} is the bandgap of material 1, and E_{G_2} is the bandgap of material 2. ΔE_C is the band discontinuity for the conduction band, and ΔE_V is the band discontinuity for the valence band. In a heterojunction based TFET, the use of III-V compound semiconductors with which a variety of bandgaps that can be designed by changing the materials and content can also be expected. Among them, InAs/Si and InAs/GaSb heterojunctions are attracting attention. An S factor of 21 mV/decade a TFET using a heterostructure of InAs/Si grown on a Si (111) substrate has been reported.[22)] On the other hand, an S factor of 48 mV/decade and an ON current of 10 μA/μm and an ON current greater than a Si MOSFET at a low gate voltage in the neighborhood of 0.2 V were reported in a TFET using a heterostructure of InAs/GaAsSb/GaSb grown on an Si (111) substrate.[27)] The device performance of heterojunction based TFETs is expected to improve by using III-V compound semiconductors. In addition, p-type TFETs are expected to be developed through the use of heterojunctions.[22),25),30)–32)]

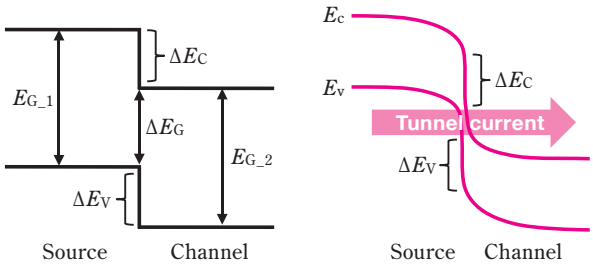

Fig. 11 Schematic illustration of the heterostructure for TFET with the effective narrow band gap

Fusion of III-V Compound Semiconductors with Si Technology

1. Integration of III-V Compound Semiconductors on 300 mm Si Substrates

The characteristics of InGaAs TFETs fabricated on InP substrates are described in the previous sections, but the diameter of InP substrates is smaller than Si substrates. The limitation of the diameter of the wafer, integration of the III-V TFET onto the Si platform and the compatibility with the conventional Si technologies are key issues to be solved for practical application. Therefore, it is important to integrate the III-V compound semiconductor channels on Si wafers. However, the differences between the characteristics of the materials of III-V compound semiconductors and Si are a problem for integration of III-V compound semiconductors on Si. When III-V compound semiconductors are adapted to the Si technology, a method for integration of III-V compound semiconductor channels on Si is important in a state where the III-V compound semiconductor devices can exhibit their performance sufficiently. There are reported methods of direct epitaxial growth,[33)–40)] methods of selective epitaxial growth,[22),25),27),32),41)–46)] and methods of wafer bonding[47)–58)] as methods for integration of III-V compound semiconductor channels on Si.

In the methods of direct epitaxial growth, it is reported that the InGaAs MOSFETs fabricated on 300 mm Si wafers showed the similar performance as the InGaAs MOSFETs fabricated on InP wafers.[37),38)] Because the integration of the III-V compound semiconductor channels on a whole 300 mm Si wafer can be feasible, incorporating III-V compound semiconductor channels into

a commercial product can be expected in the future.

With the methods of selective epitaxial growth, it is possible to form III-V compound semiconductor channels at any location even though processes of a Si wafer are necessary.[22),25),27),32),41)–46)] It is possible to integrate different channel materials, and channel shape can be controlled by process conditions. Therefore, there are expectations for developments in the future.

Wafer bonding is a method for transferring an epitaxial layer grown on a III-V compound semiconductor wafer to a Si substrate with good crystallinity. Fabrication of an InGaAs-on-insulator (InGaAs-OI) wafer with good crystallinity is possible using direct wafer bonding (DWB).[47)–51)] Here, the InGaAs-OI wafer has a structure in which the InGaAs channel is integrated via a buried oxide film on a Si wafer. On the other hand, the small diameter of the semiconductor wafer forming the transfer wafer is an issue with fabricating the large-diameter InGaAs-OI wafers. It can be solved by a method of transferring a III-V compound semiconductor layer grown directly on a large-diameter Si wafer to a large-diameter transfer destination Si wafer using DWB, and this method is explained in **Fig. 12**.[55),56)] First, an InGaAs epitaxial wafer is fabricated by growth of an InGaAs epitaxial layer on a large-diameter Si wafer, which is used for transfer of an InGaAs channel layer. In the fabrication of an InGaAs epitaxial wafer, a GaAs buffer layer is first grown on a Si wafer, an InAlAs buffer layer is subsequently grown on the GaAs buffer layer, and an InGaAs layer is finally grown on the InAlAs/GaAs buffer layer (**Fig. 12**-a). Here, the InAlAs/GaAs buffer layer can contribute to the improvement of the crystallinity of the InGaAs channel layer. Next, Al_2O_3 films are formed on the surfaces of the InGaAs epitaxial wafer and the transfer destination Si wafer by atomic layer deposition (ALD). In case the surface roughness of the transfer InGaAs wafers is not enough to perform DWB, the surface of the Al_2O_3 layer deposited on the transfer InGaAs wafer is made to be smooth enough to perform DWB by chemical mechanical polishing (CMP) (**Fig. 12**-b). Thereafter, DWB is carried out using the transfer and transfer destination wafers with the smooth surfaces (**Fig. 12**-c). Finally, the transfer Si wafer and InAlAs/GaAs buffer layer are eliminated from the transfer InGaAs channel layer, and the large-diameter InGaAs-OI wafer is completed by forming the InGaAs channel layer via the Al_2O_3 layer on the transfer destination Si wafer (**Fig. 12**-d). It is possible to fabricate large-diameter InGaAs-OI wafers by using 300 mm Si substrates in this method.

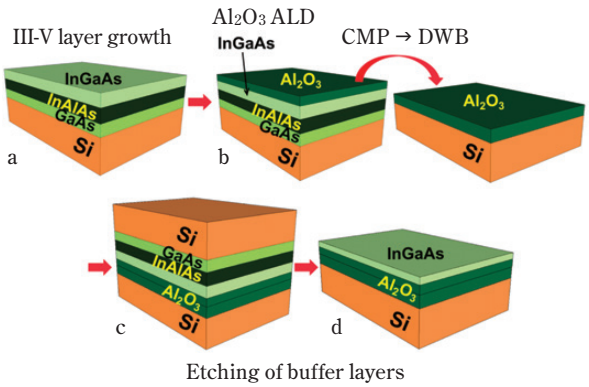

Fig. 12 Schematic illustration of fabrication of InGaAs-OI wafer by developed DWB techniques using Si donor wafer with 300 mm scalability
Figure created by using data provided by collaborators (Ref. 9, 55, 56)

As another method for increasing the diameter and speed of fabrication of the III-V compound semiconductors on Si wafers, a wafer fabrication method using epitaxial lift-off (ELO) has been developed. The ELO method is as follows. First, the III-V compound semiconductor channel layer is formed on the transfer wafers. Subsequently, the transfer wafers are bonded to the 300 mm Si transfer destination wafers. Finally, the III-V compound semiconductor channel layers are released from the transfer wafers using ELO.[57),58)] Here, GaAs wafers are used as the transfer wafers. After an AlAs layer for selective etching by ELO is grown on the GaAs wafer, a GaAs channel layer is grown on the AlAs etching sacrificial layer. Periodic patterns are formed on the GaAs/AlAs layer in order to perform ELO, and ELO of the GaAs layer is carried out by selective etching of the AlAs layer using an HCl solution. It has been confirmed that the surface roughness of the channel layer transferred onto the Si wafer is as smooth as 0.4 nm. **Fig. 13** shows a photograph of GaAs layers transferred onto a 300 mm Si wafer using

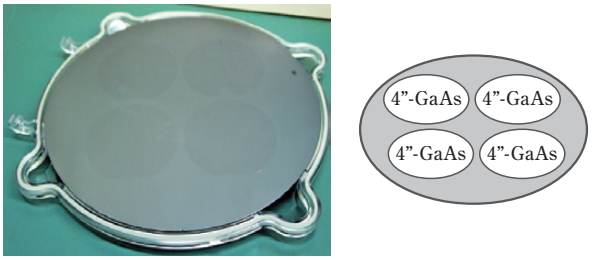

Fig. 13 Photograph of GaAs on 300 mm Si wafer [57)]

ELO. The diameter of the transferred GaAs layers is 100 mm. It has been confirmed that the GaAs layer maintains high crystal quality after the transfer onto the Si wafer as evaluated by x-ray diffraction measurements and photoluminescence measurements. Wafer bonding can be adapted to the transfer of the various types of materials, and it is possible to form channels in the necessary regions. Therefore, development of a method for the integration of different types of materials on the identical wafer is expected.

2. Development of Technology for Ultra-low Power Consumption

For the development of even lower power consuming devices, development and integration optical devices using III-V/Si hybrid structures is expected.[59)–61)] It is possible to achieve superior performance in optical devices with III-V compound semiconductors compared to those with Si. The integration of III-V compound semiconductor optical devices can allow us to realize systems with much less power consumption than conventional systems.

In terms of devices making use of the characteristics of III-V compound semiconductors, a great deal of research and development has been done on vertical cavity surface emitting lasers (VCSEL), terahertz devices, and so on. VCSEL is used for optical communications and sensing, and there are expectations for their being applied to automotive applications. For terahertz devices, high electron mobility transistors (HEMTs) with InGaAs and InAs channels, MOSHEMT, quantum cascade lasers, resonant tunneling diodes, and so on have attracted much attention, and it is expected that applications for communications, sensing, security, medicine, and so on can be realized. As described above, there are expectations for dramatic improvements in bringing multi-functionalization to mobile devices by the integration of devices with different functions and ultra-low power consuming circuits.

As we have discussed in this paper, it has been verified that operable circuits with ultra-low power consumption can be achieved by the use of low power consuming devices with new structures using compound semiconductors, and the use of integration technologies for materials and devices on large-diameter wafers.

We hope that various types of applications and services based on communication and sensing technology in a variety of terminals can become possible and make a contribution to the development of society through the development of low power consumption technologies for devices.

Acknowledgments

In the bringing together this paper, we would like to express our gratitude to Prof. Shinichi Takagi and Assoc. Prof. Mitsuru Takenaka of the Department of Electrical and Nearing Information Systems, Graduate School of Engineering, The University of Tokyo for providing data and for their beneficial advice.

References

1) International Roadmap for Devices and Systems, “INTERNATIONAL ROADMAP FOR DEVICES AND SYSTEMS 2016 EDITION MORE MOORE WHITE PAPER”, http://irds.ieee.org/images/files/pdf/2016_MM.pdf (Ref. 2017/5/19).
2) S. Takagi, R. Zhang, J. Suh, S.-H. Kim, M. Yokoyama, K. Nishi and M. Takenaka, *Jpn. J. Appl. Phys.*, **54**, 06FA01 (2015).
3) J. A. del Alamo, *Nature*, **479**, 317 (2011).
4) R. Pillarisetty, *Nature*, **479**, 324 (2011).
5) A. C. Seabaugh and Q. Zhang, *Proc. IEEE*, **98**, 2095 (2010).
6) A. M. Ionescu and H. Riel, *Nature*, **479**, 329 (2011).
7) H. Lu and A. Seabaugh, *J. Electron Devices Soc.*, **2**, 44 (2014).
8) S. Takagi, D. H. Ahn, M. Noguchi, T. Gotow, K. Nishi, M. Kim and M. Takenaka, *IEDM Tech. Dig.*, **2016**, 516.
9) S. Takagi, M. Noguchi, M. Kim, S.-H. Kim, C.-Y. Chang, M. Yokoyama, K. Nishi, R. Zhang, M. Ke and M. Takenaka, *Solid-State Electronics*, **125**, 82 (2016).
10) G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then and R. Chau, *IEDM Tech. Dig.*, **2011**, 785.
11) M. Noguchi, S. H. Kim, M. Yokoyama, S. M. Ji, O. Ichikawa, T. Osada, M. Hata, M. Takenaka and S. Takagi, *IEDM Tech. Dig.*, **2013**, 683.
12) M. Noguchi, S. H. Kim, M. Yokoyama, O. Ichikawa, T. Osada, M. Hata, M. Takenaka and S. Takagi, *J. Appl. Phys.*, **118**, 045712 (2015).
13) D. H. Ahn, S. M. Ji, M. Takenaka and S. Takagi, *Symp. VLSI Tech. Dig.*, **2016**, 224.

14) Ioffe Physico-Technical Institute, Electronic archive New Semicondutor Materials. Characteristics and Properties, http://www.ioffe.rssi.ru/SVA/NSM/ (Ref. 2017/5/19).
15) S. H. Kim, M. Yokoyama, N. Taoka, R. Iida, S. Lee, R. Nakane, Y. Urabe, N. Miyata, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Takenaka and S. Takagi, *IEDM Tech. Dig.*, **2010**, 596.
16) A. Alian, J. Franco, A. Vandooren, Y. Mols, A. Verhulst, S. El Kazzi, R. Rooyackers, D. Verreck, Q. Smets, A. Mocuta, N. Collaert, D. Lin and A. Thean, *IEDM Tech. Dig.*, **2015**, 823.
17) A. Alian, Y. Mols, C. C. M. Bordallo, D. Verreck, A. Verhulst, A. Vandooren, R. Rooyackers, P. G. D. Agopian, J. A. Martino, A. Thean, D. Lin, D. Mocuta and N. Collaert, *Appl. Phys. Lett.*, **109**, 243502 (2016).
18) T. Sato, M. Mitsuhara and Y. Kondo, "NTT Technical Review, January 2009 Vol. 7 No. 1", https://www.ntt-review.jp/archive/ntttechnical.php?contents=ntr200901sf2.html (Ref. 2017/5/19).
19) J. W. Matthews and A. E. Blakeslee, *J. Cryst. Growth*, **27**, 118 (1974).
20) R. People and J. C. Bean, *Appl. Phys. Lett.,* **47**, 322 (1985).
21) A. Fischer, H. Kühne and H. Richter, *Phys. Rev. Lett.*, **73**, 2712 (1994).
22) K. Tomioka, M. Yoshimura and T. Fukui, *Symp. VLSI Tech. Dig.*, **2012**, 47.
23) U. E. Avci and I. A. Young, *IEDM Tech. Dig.*, **2013**, 96.
24) R. Pandey, N. Agrawal, V. Chobpattana, K. Henry, M. Kuhn, H. Liu, M. Labella, C. Eichfeld, K. Wang, J. Maier, S. Stemmer, S. Mahapatra and S. Datta, *IEDM Tech. Dig.*, **2015**, 354.
25) D. Cutaia, K. E. Moselund, H. Schmid, M. Borg, A. Olziersky and H. Riel, *Symp. VLSI Tech. Dig.*, **2016**, 226.
26) T. Gotow, M. Mitsuhara, T. Hoshi, H. Sugiyama, M. Takenaka and S. Takagi, *Ext. Abstr. Solid State Devices and Materials*, **2016**, 21.
27) E. Memisevic, J. Svensson, M. Hellenbrand, E. Lind and L.-E. Wernersson, *IEDM Tech. Dig.*, **2016**, 501.
28) A. Afzalian, M. Passlack and Y-. C. Yeo, *IEDM Tech. Dig.*, **2016**, 738.
29) I. A. Young, U. E. Avci and D. H. Morris, *IEDM Tech. Dig.*, **2015**, 600.
30) R. Pandey, H. Madan, H. Liu, V. Chobpattana, M. Barth, B. Rajamohanan, M. J. Hollander, T. Clark, K. Wang, J.-H. Kim, D. Gundlach, K. P. Cheung, J. Suehle, R. Engel-Herbert, S. Stemmer and S. Datta, *Symp. VLSI Tech. Dig.*, **2015**, T206.
31) R. Pandey, C. Schulte-Braucks, R. N. Sajjad, M. Barth, R. K. Ghosh, B. Grisafe, P. Sharma, N. von den Driesch, A. Vohra, B. Rayner, R. Loo, S. Mantl, D. Buca, C.-C. Yeh, C.-H. Wu, W. Tsai, D. Antoniadis and S. Datta, *IEDM Tech. Dig.*, **2016**, 520.
32) H. Schmid, D. Cutaia, J. Gooth, S. Wirths, N. Bologna, K. E. Moselund and H. Riel, *IEDM Tech. Dig.*, **2016**, 71.
33) Y.-C. Lin, M.-L. Huang, C.-Y. Chen, M.-K. Chen, H.-T. Lin, P.-Y. Tsai, C.-H. Lin, H.-C. Chang, T.-L. Lee, C.-C.. Lo, S.-M. Jang, C. H. Diaz, H.-Y. Hwang, Y.-C. Sun and E. Y. Chang, *Appl. Phys. Express*, **7**, 041202 (2014).
34) T. Orzali, A. Vert, R. T. P. Lee, A. Norvilas, G. Huang, J. L. Herman, R. J. W. Hill and S. S. Papa Rao, *J. Cryst. Growth*, **426**, 243 (2015).
35) T. Orzali, A. Vert, T.-W. Kim, P. Y. Hung, J. L. Herman, S. Vivekanand, G. Huang, M. Kelman, Z. Karim, R. J. W. Hill and S. S. Papa Rao, *J. Cryst. Growth*, **427**, 72 (2015).
36) T. Orzali, A. Vert, B. O'Brien, J. L. Herman, S. Vivekanand, R. J. W. Hill, Z. Karim and S. S. Papa Rao, *J. Appl. Phys.*, **118**, 105307 (2015).
37) M. L. Huang, S. W. Chang, M. K. Chen, C. H. Fan, H. T. Lin, C. H. Lin, R. L. Chu, K. Y. Lee, M. A. Khaderbad, Z. C. Chen, C. H. Lin, C. H. Chen, L. T. Lin, H. J. Lin, H. C. Chang, C. L. Yang, Y. K. Leung, Y.-C. Yeo, S. M. Jang, H. Y. Hwang and Carlos H. Diaz, *Symp. VLSI Tech. Dig.*, **2015**, T204.
38) M. L. Huang, S. W. Chang, M. K. Chen, Y. Oniki, H. C. Chen, C. H. Lin, W. C. Lee, C. H. Lin, M. A. Khaderbad, K. Y. Lee, Z. C. Chen, P. Y. Tsai, L. T. Lin, M. H. Tsai, C. L. Hung, T. C. Huang, Y. C. Lin, Y.-C. Yeo, S. M. Jang, H. Y. Hwang, Howard C.-H. Wang and C. H. Diaz, *Symp. VLSI Tech. Dig.*, **2016**, 16.
39) R. Alcotte, M. Martin, J. Moeyaert, R. Cipro, S. David, F. Bassani, F. Ducroquet, Y. Bogumilowicz, E. Sanchez, Z. Ye, X. Y. Bao, J. B. Pin and T. Baron, *APL Materials*, **4**, 046101 (2016).
40) M. Martin, D. Caliste, R. Cipro, R. Alcotte, J. Moeyaert, S. David, F. Bassani, T. Cerba, Y. Bogumilowicz, E. Sanchez, Z. Ye, X. Y. Bao, J. B. Pin, T. Baron and P. Pochet, *Appl. Phys. Lett.*, **109**, 253103 (2016).
41) N. Waldron, S. Sioncke, J. Franco, L. Nyns, A. Vais, X. Zhou, H. C. Lin, G. Boccardi, J. W. Maes, Q. Xie,

M. Givens, F. Tang, X. Jiang, E. Chiu, A. Opdebeeck, C. Merckling, F. Sebaai, D. van Dorp, L. Teugels, A. S. Hernandez, K. D. Meyer, K. Barla, N. Collaert and Y-V. Thean, *IEDM Tech. Dig.*, **2015**, 799.

42) X. Zhou, N. Waldron, G. Boccardi, F. Sebaai, C. Merckling, G. Eneman, S. Sioncke, L. Nyns, A. Opdebeeck, J. W. Maes, Q. Xie, M. Givens, F. Tang, X. Jiang, W. Guo, B. Kunert, L. Teugels, K. Devriendt, A. Sibaja Hernandez, J. Franco, D. van Dorp, K. Barla, N. Collaert and A. V-Y. Thean, *Symp. VLSI Tech. Dig.*, **2016**, 166.

43) L. Czornomaz, E. Uccelli, M. Sousa, V. Deshpande, V. Djara, D. Caimi, M. D. Rossell, R. Erni and J. Fompeyrine, *Symp. VLSI Tech. Dig.*, **2015**, T172.

44) H. Schmid, M. Borg, K. Moselund, L. Gignac, C. M. Breslin, J. Bruley, D. Cutaia and H. Riel, *Appl. Phys. Lett.*, **106**, 233101 (2015).

45) L. Czornomaz, V. Djara, V. Deshpande, E. O'Connor, M. Sousa, D. Caimi, K. Cheng and J. Fompeyrine, *Symp. VLSI Tech. Dig.*, **2016**, 94.

46) M. Borg, H. Schmid, J. Gooth, M. D. Rossell, D. Cutaia, M. Knoedler, N. Bologna, S. Wirths, K. E. Moselund and H. Riel, *ACS Nano*, **11**, 2554 (2017).

47) M. Yokoyama, M. Takenaka, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano and S. Takagi, *Symp. VLSI Tech. Dig.*, **2009**, 242.

48) M. Yokoyama, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka and S. Takagi, *Appl. Phys. Express*, **2**, 124501 (2009).

49) M. Yokoyama, T. Yasuda, H. Takagi, N. Miyata, Y. Urabe, H. Ishii, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka and S. Takagi, *Appl. Phys. Lett.*, **96**, 142106 (2010).

50) M. Yokoyama, R. Iida, S. H. Kim, N. Taoka, Y. Urabe, T. Yasuda, H. Takagi, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka and S. Takagi, *IEDM Tech. Dig.*, **2010**, 46.

51) M. Yokoyama, R. Iida, S.-H. Kim, N. Taoka, Y. Urabe, H. Takagi, T. Yasuda, H. Yamada, N. Fukuhara, M. Hata, M. Sugiyama, Y. Nakano, M. Takenaka and S. Takagi, *IEEE Electron Device Lett.*, **32**, 1218 (2011).

52) T. Irisawa, M. Oda, Y. Kamimuta, Y. Moriyama, K. Ikeda, E. Mieda, W. Jevasuwan, T. Maeda, O. Ichikawa, T. Osada, M. Hata and T. Tezuka, *Symp. VLSI Tech. Dig.*, **2013**, T56.

53) T. Irisawa, M. Oda, K. Ikeda, Y. Moriyama, E. Mieda, W. Jevasuwan, T. Maeda, O. Ichikawa, T. Osada, M. Hata, Y. Miyamoto and T. Tezuka, *IEDM Tech. Dig.*, **2013**, 28.

54) T. Irisawa, K. Ikeda, Y. Moriyama, M. Oda, E. Mieda, T. Maeda and T. Tezuka, *Symp. VLSI Tech. Dig.*, **2014**, 118.

55) S. H. Kim, Y. Ikku, M. Yokoyama, R. Nakane, J. Li, Y. C. Kao, M. Takenaka and S. Takagi, *Symp. VLSI Tech. Dig.*, **2014**, T32.

56) S. H. Kim, Y. Ikku, M. Yokoyama, R. Nakane, J. Li, Y.-C. Kao, M. Takenaka and S. Takagi, *Appl. Phys. Lett.*, **105**, 043504 (2014).

57) E. Mieda, T. Maeda, N. Miyata, T. Yasuda, Y. Kurashima, A. Maeda, H. Takagi, T. Aoki, T. Yamamoto, O. Ichikawa, T. Osada, M. Hata, A. Ogawa, T. Kikuchi and Y. Kunii, *Jpn. J. Appl. Phys.*, **54**, 036505 (2015).

58) T. Maeda, E. Mieda, H. Ishii, T. Itatani, H. Hattori, T. Yasuda, A. Maeda, Y. Kurashima, H. Takagi, T. Aoki, T. Yamamoto, O. Ichikawa, T. Osada, T. Takada, M. Hata, J. Yugami, A. Ogawa, T. Kikuchi and Y. Kunii, *ECS Transactions*, **64** (6) 491 (2014).

59) A. W. Fang, H. Park, O. Cohen, R. Jones, M. J. Paniccia and J. E. Bowers, *Opt. Express*, **14** (20), 9203 (2006).

60) M. Takenaka, M. Yokoyama, M. Sugiyama, Y. Nakano and S. Takagi, *Appl. Phys. Express.*, **2**, 122201 (2009).

61) J.-H. Han, M. Takenaka and S. Takagi, *IEDM Tech. Dig.*, **2016**, 620.

PROFILE

Masafumi YOKOYAMA

Sumitomo Chemical Co., Ltd.
IT-related Chemicals Research Laboratory
Researcher, Ph. D.

Taketsugu YAMAMOTO

Sumitomo Chemical Co., Ltd.
IT-related Chemicals Research Laboratory
Senior Research Associate