Epitaxial Growth of Compound Semiconductors Using MOCVD (IV)

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GaAs based compound semiconductors have been widely used for mobile applications in devices, such as smartphones, tablet PCs, base stations, and so on, because of their superior RF properties.

One of their major applications is the FEMs (Front-End Modules) of mobile phones, and InGaP-HBT which is suitable for power amplifiers in FEMs has been developed. In this paper InGaP-HBT epitaxial wafer fabrication techniques using MOCVD growth method are reviewed.

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Introduction

In recent years, there has been an increase in the amount of communications data because of cloud computing and other activities using mobile communications devices typified by mobile phones and the handling of increased data speeds for data communications. With the dissemination of LTE (Long Term Evolution) as a communication mode, progress has been made with multiband frequencies, and the number of bands, which was 2 to 3 before 2G, has increased to 10 bands or more. In addition, applications other than mobile phones have recently been frequently equipped with wireless LAN communication functions, and progress is being made in increasing the performance of the various electronic modules that run these communication processes. As a part of this, progress has been made in integrating various semiconductor devices that were discrete devices up to now to reduce the size and power consumption of RF front-end modules which receive and transmit RF-signal for communications. The front-end modules for smart phones, etc. use power amplifiers with integrated duplexers (PAiD) or front-end modules with integrated duplexers (FEMiD), etc. into which duplexers have been integrated as shown in **Fig. 1**. Among the RF front-end modules that have diversified in this manner, power amplifier modules which amplify output signals for multiple bands require high linearity in the amplification characteristics for each band. In addition, the power consumption is the greatest for power amplifier modules which process the largest signal in the device, and the power consumption tends to increase even more because of modulation systems becoming more complicated, so then even higher power efficiency is required.

Currently, electronic devices that are made of Si, SiGe, GaAs and other semiconductor materials are

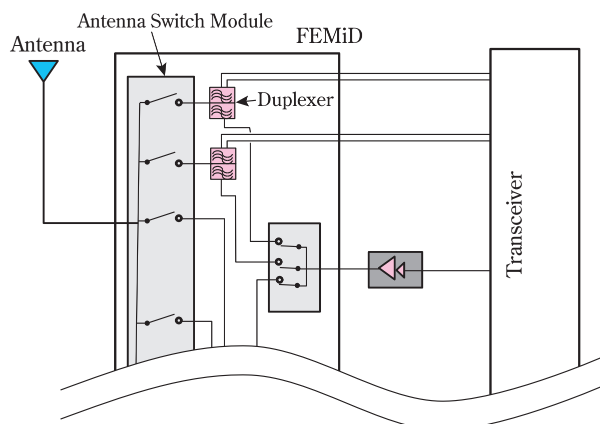

Fig. 1 Schematic diagram of front-end module in smartphones (example)

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used for the various devices in front-end modules, but among them, devices made of GaAs have the characteristics of high linearity and low power consumption, making them suitable for the power amplifier applications described above. Pseudomorphic high electron mobility transistors (p-HEMT), which are used in the antenna switches and low-noise amplifiers in front-end modules, are representative of high frequency devices that make use of GaAs semiconductors. Technical overviews of the development of these p-HEMTs have been provided in this publication several times.[1)–3)] On the other hand, heterojunction bipolar transistors (HBT) have especially excellent characteristics for power amplifier applications, as will be discussed in the following, and are widely used today. In addition, the markets for these are expanding rapidly, so this report will review the technical development of GaAs-HBT.

Principles and Characteristics of HBT

Fig. 2 shows a typical HBT structure. The most important difference from a field effect transistor, represented by p-HEMT used in a switch, is the current path, and while p-HEMT has current flowing in parallel to the surface on the substrate, HBT has current flowing vertically. With this system, an overwhelmingly larger current path cross-section can be had than with p-HEMT in which electrons flow in a thin film quantum well channel width in the tens of nanometers, and these are suitable for power amplifier applications for controlling large currents.[4)] In addition, from a different point of view, there can be a greater amount of current per device surface area; therefore, it can be said that device sizes can be shrunk, and this is one important merit of HBT in applications for mobile terminals, which have strong requirements for reduction in mounting surface area and volume. Looking at this in terms of control systems for output power, high current density can be assured from a so-called normally-on type p-HEMT where a settled current flows when the gate voltage is zero, but two power supplies, positive and negative, are required between operating amplitudes during maximum current output (positive gate voltage) and during shut-off (negative gate voltage). A shut-off state with a gate voltage of zero, where current increases and reductions are only controlled by a positive gate voltage, a so-called normally-off type, is also possible, but the effective channel charge density becomes smaller; therefore, current density decreases, and there is the disadvantage of the device area increasing in order to assure the required output current. On the other hand, with HBT, the current polarity necessary for the control of the base current signal and the current polarity applied to the collector are the same; therefore, there is the advantage of drive being possible with a single power supply, and salient features are the ability to simplify power supply voltage circuits coupled with higher current density per unit surface area than conventionally, and the ability to form power amplifiers which are small and which can control high current outputs.

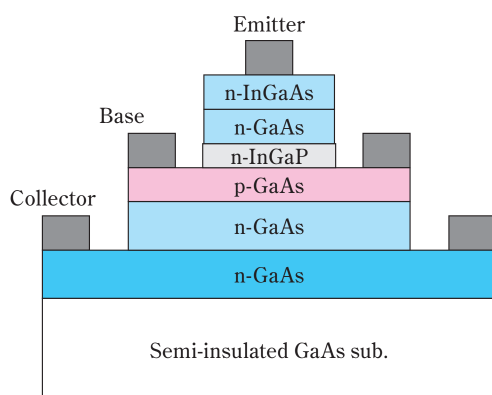

Fig. 2 Typical HBT (Heterojunction Bipolar Transistor) structure

Next, the band structure of the crystals forming HBT will be discussed. With compound semiconductors such as GaAs and InP, a variety of band lineups can be designed by forming heterojunctions using alloy crystals. For example, a discontinuous band structure can be fabricated by stacking AlGaAs or InGaP, which have a large band gap, on a GaAs semiconductor while matching the lattice constant. In addition, with AlGaAs and InGaP, the energy difference differs from the vacuum level at the lower end of the conduction band and the upper end of the valence band; therefore, a suitable band lineup can be created according to the purpose by combining them, and they are frequently used in electronic and optical devices. As will be described in the following, an emitter layer formed from AlGaAs or InGaP, which have a large band gap, is formed adjacent to a base layer formed from GaAs with HBT so that a high energy barrier is formed between the valence band of the base layer and the valance band of the emitter layer, and diffusion of minority carriers injected from the base layer into the emitter layer can be suppressed. Thus, current loss during the driving of the transistor can be reduced, and a high current gain can be achieved.

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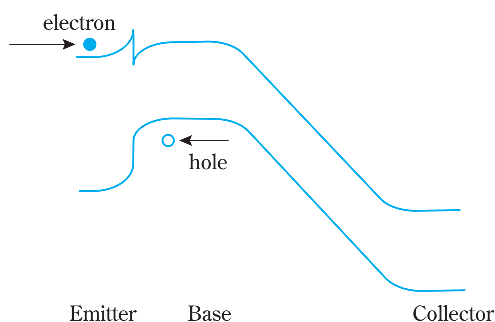

Fig. 3 Band structure of HBT

Most group Ⅲ–V compound semiconductors, starting with the GaAs material described here, have high electron transport velocity; therefore, electrons are used as the majority carrier in most of the electronic devices. For example, while p-HEMT makes for monopolar devices that only control current with electrons, a npn structure where electrons, which have high electron transport velocity, are used as the majority carrier is typical in HBT, but holes must also be controlled along with the electrons as a signal source, and not only n type but also p type crystal growth control is necessary. A typical HBT band structure is shown in **Fig. 3**. When no voltage is applied to the base, electrons are not injected from the emitter into the base because of the energy barrier at the pn junction formed between the emitter and the base, even when the collector is positively biased to the emitter, but when a positive voltage is applied to the base, then electrons are injected into the base from the emitter. Some of the electrons injected from the emitter recombine with holes that have been injected into the base layer at the emitter/base interface, and a hole recombination current I_{Br} is formed. Electrons that do not recombine flow into the collector as-is, and form a collector current I_C. On the other hand, some of the holes in the base layer are reverse injected into the emitter layer and form a reverse injection base current I_{Bh}. Therefore the base current of the transistor is expressed by

$$I_B = I_{Br} + I_{Bh}$$

and the current gain β, which is the ratio of the base current and the collector current, is expressed by the following equation.

$$\beta = \frac{I_C}{I_B} = \frac{I_C}{I_{Br} + I_{Bh}}$$

With HBT there is a greater valence band barrier between the emitter and the base than with a homojunction bipolar transistor; therefore, it is possible to make I_{Bh} smaller, and it is possible to obtain a high β value.

In addition, the maximum cutoff frequency f_T, which is an index of the highest frequency for current amplification, is inversely proportional to the sum of the electron transit time in the base layer and collector layer; therefore, the appropriate structural design is required for the HBT operation at high frequencies.[4] Specifically, f_T can be increased by applying a thinner base layer or by accelerating electrons with a structure that applies an electric field inside the base layer. In addition, f_{max}, which is an index of highest frequency for the power gain, is known to be dependent on capacitance between the base and the collector and the base resistance. Therefore, it is essential to have good crystallinity, high doping concentration and low base resistance for the base layer to improve f_T and f_{max}.

MOCVD Grown HBT Epitaxial Crystals

Crystal growth control for p-HEMT using MOCVD has previously been reported in this publication. The basic MOCVD growth technology is also common to HBT growth, and the technology is used in the same way, but the crystal materials are different, and the current control methods in devices are also different; therefore, growth technology which is different from p-HEMT must be used. In the following we will describe the relationship between the growth technology and device characteristics.

1. Growth of p type GaAs crystals and initial drift phenomena in current drive

A p-type GaAs layer is typically used in the base layer for GaAs-HBT. When growing p-type GaAs, group Ⅱ elements such as Be, Mg and Zn or group Ⅳ elements such as C are doped as the acceptors.[5] Typically group Ⅱ dopants are suitable for obtaining high p-type carrier concentrations, and they are used in optical applications such as lasers and LED electrode contact layers; however, there is the problem of the diffusion speed being high within the crystals, and so they are not suited for HBT, which requires high concentrations and a steep doping profile. If mutual diffusion of dopants in HBT interfaces arises at a pn junction, they compensate for each other. Since ionized impurity concentration increases within the crystals with the occurrence

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of this compensation of dopants for each other, it invites a reduction in mobility, in other words, a reduction in the electron transport velocity. In addition, in heterojunction materials, the design of crystal composition interfaces and pn junction interfaces must be consistent, but when impurity diffusion arises, it gives rise to offsetting of pn junction interfaces or degradation. Important device parameters such as transistor turn-on voltage vary, and since there is a serious effect on their operating characteristics and reliability, a steep doping profile without mutual diffusion is necessary. Because of this, C, which has an extremely small diffusion coefficient, is suitable as an acceptor element for the base layer. Besides halomethane gases such as CBr_4 and $CBrCl_3$, organic arsenic gases such as trimethyl As and tertiary butyl As, which can also be used as As sources, can be used as the dopant sources for doping with C. In addition, when trimethylgallium is used as a Ga source, it can also be used as a source of C, making use of the phenomenon of C being naturally incorporated into the crystal from its methyl groups. Typically, from the standpoint of assuring crystallinity and film thickness controllability, crystal growth is most often carried out while strictly controlling the Ga source flow rate under Ga source material supply rate limiting conditions while supplying an excess of As, which has a large decomposition and dissociation pressure, when carrying out GaAs growth using MOCVD. Therefore, cases using halomethane doping where the amount of C doping can be controlled independently from the As and Ga source materials, which also require strict control from the standpoint of these crystal controls, are common.[6)]

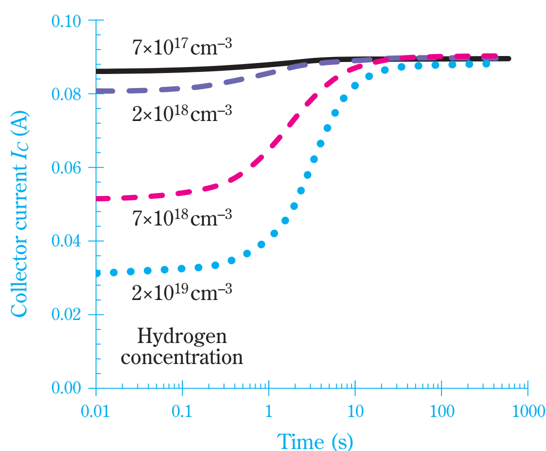

Fig. 4 Initial collector current drift (Burn-in effect)

However, there are also problems that arise when growing p-type GaAs crystals using C as a dopant. Typically, the maximum carrier concentration obtained is known to be dependent on the energy band structure inherent in the semiconductor material in electrical conductivity control using doping in semiconductor crystals. Specifically, the lower end of the conduction band and the energy difference at a charge neutrality level with n-type doping are known from experiments to have a strong correlation with empirical values for maximum carrier concentration obtained in various semiconductor materials. The maximum carrier concentration for a given semiconductor material can be thought of being determined largely by the relative position of the neutrality level in the band structure of that semiconductor material and the conduction band and valence band positions.[7)] When the dopant is supplied in a greater amount than the maximum carrier concentration determined by this band structure, the dopant atoms are taken into the crystal, but by introducing defects, etc., that compensate for this into the crystal, it can move to a stable energy state. In terms of these defects, ones caused by the formation of vacancies and interstitial atoms as well as complexes of those defects can be cited, but when doping with C is carried out in GaAs crystals by MOCVD, H is taken up in the crystal and bonds with C, compensating for the C acceptors. Thus, if HBT with a C-doped GaAs crystal as the base layer is fabricated, the device operation is affected by H compensating for the C acceptors. This is what is called the burn-in effect,[8)] and when the HBT turns on, changes in the C-H bond state arise because of the electrical and thermal stress, and the C acceptor compensation by H is partly eliminated. As a result, the effective carrier concentration of the base layer changes, and as a result of that the collector current and current gain change (**Fig. 4**). The concentration of H atoms in the p-GaAs crystal must be kept low in advance to control these changes in characteristics with initial turning on of the device, and typically, an in-situ post annealing process is used after C-doped GaAs layer growth. Even when high concentration p-type GaAs with a p-type carrier concentration of around $4 \times 10^{19} cm^{-3}$ is used for the base layer, the H concentration of greater than $7 \times 10^{18} cm^{-3}$ right after base layer growth can be reduced to less than or equal to $7 \times 10^{17} cm^{-3}$ by applying the post annealing process, and the collector current variations in initial operation of the device after turning on can be suppressed. By

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using p-type GaAs base layers that make use of these C acceptors, practically acceptable performance for current mobile communications for the f_T and f_{max} values described above have been achieved. This method of using post annealing carries out C doping at a high concentration while maintaining the energy difference between the charge neutrality level and the upper end of the valence band by inactivating with H during the crystal growth, and is an extremely effective method because it is able to obtain a high carrier concentration not normally achieved by MOCVD growth conditions close to thermal equilibrium by activating the C in the post annealing process after growth. In this connection, there is the example of success in p-type carrier activation and increased concentration that exceed by far the maximum doping carrier concentration predicted from the band structure previously described by separating hydrogen by post growth annealing of Mg acceptors that have been deactivated by hydrogen during growth using a similar method with an Mg-doped GaN layer used as a p-type layer in blue light-emitting devices, which received the Nobel prize in 2014.

As described above, there are two methods for C doping in GaAs, and one is the method of introducing a CBr_4 or $CBrCl_3$ from the outside, and the other is adjusting the supply ratio of trimethylgallium (TMG, $Ga(CH_3)_3$) and arsine (AsH_3), which are the constituent raw materials for Ga and As, that is the V/Ⅲ ratio. We have discovered technology for controlling the current amplification factor in HBT by adjusting the V/Ⅲ ratio and, by reducing the hydrogen concentration taken into the crystal, have achieved device characteristics that sufficiently reduce the burn-in effect.

2. HBT characteristics and relationship with high concentration n-type doping in crystals

During operation, HBT devices can be thought of as a type of resistance element. From the standpoint of reducing power loss, it is important to lower the resistance of the various HBT layers and also to reduce contact resistance in the forming of electrodes, which are the external output terminals for the main layers constituting HBT. To achieve this, selection of suitable electrode materials and epitaxial design are required. The main point is lowering the energy barrier between the electrodes and the semiconductor as much as possible in the epitaxial design. The contact resistance is reduced by the high p-type carrier concentration doping technology described above for the base layer, but contact resistance must be lowered similarly for the collector layer formed from the n-type GaAs layer and the emitter layer formed from the n-type InGaAs layer. In particular, formation of an electrode surface area that is very much smaller than the collector electrode and base electrode, which have comparatively large surface areas, is necessary for the emitter; therefore, the reduction of the contact resistance of the electrode, which increases in inverse proportion to the electrode surface area and reduction of the resistance in the vertical direction of the emitter layer to the base are important problems to be solved. A method for forming ohmic contact on a GaAs compound semiconductor is by forming a film by vapor deposition, etc., of an electrode material that includes dopant elements and the dopant elements being diffused in the crystal by carrying out heat treatment afterward, forming a high carrier concentration region and reducing the contact resistance. This diffusion technology is commonly used in source and drain electrodes for horizontal-type devices such as field effect transistors (FETs), but in HBT, which is a vertical device, the diffusion of dopant elements may affect the transistor operation. Specifically, the carrier concentration may vary between the base layer and the emitter layer for which carrier concentration control should be carried out if diffusion processing is carried out on the emitter layer formed on the outermost epitaxial layer, and by extension, the response characteristics when the bias voltage between the base and emitter is changed in comparison to the original design values. Therefore, it is preferable to be able to achieve low contact resistance in emitter electrodes without diffusion by heat treatment, and use of materials with small energy barriers and high carrier concentration doping that makes barrier tunneling possible is effective. InGaAs with a high In composition is an emitter contact layer material with a small energy barrier. As the In composition in InGaAs increases, the electron affinity becomes larger, and the energy barrier for electron injection is reduced. In addition, an important merit is the ability to obtain a much higher doping concentration than GaAs because of the band structure characteristics described previously. However, since the lattice constants for InGaAs and GaAs differ, defects are easily introduced into the crystal by lattice mismatch. The emitter contact layer is positioned as the topmost part in the HBT structure, and even though there is no problem with propagation of crystal defects above that, layer structure design and growth

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conditions must be optimized to be able to form a layer with few crystal defects, because the effects of the defect level when the layer is formed lead to current loss when there are too many of these crystal defects. Si, Ge, S, Sn, Se and Te are used as donor elements in n-type high concentration doping of InGaAs emitter contact layers, and doping with high concentrations greater than $2\times10^{19}cm^{-3}$ is possible. A low ionization energy for a donor element is desirable from the standpoint of donor activation, but on the other hand, use of dopant sources having the characteristic of releasing when adsorbed on the walls and other parts of the reactor becomes a problem from the standpoint of mass production stability. It can be said that Si, which has little adsorption and desorption effect and can form a steep doping profile, is suitable for mass production.

On the other hand, use of a GaAs layer for the contact layer on the collector side is typical. One reason for using the GaAs contact layer is that there is no current pathway for transistor operation below the collector contact layer and diffusion treatment of the electrode is possible. Another reason is that the growth of a high quality GaAs epitaxial layer on the InGaAs contact layer is difficult because the difference in lattice constant between InGaAs and GaAs is large, and dislocations are introduced in the GaAs layer. This is different from the emitter contact layer which is positioned at the uppermost epitaxial part. However, even in the collector contact layer, where electrode diffusion can be used, high carrier concentration doping is required to a certain extent. This is not only because of the contact resistance with the electrode, but also for reducing the series resistance component in the path of electron flow horizontally from the electrode. The maximum carrier concentration that can be obtained with n-type high carrier concentration doping of GaAs is lower than that for the p-type at less than $1\times10^{19}cm^{-3}$. This is because the lower end of the GaAs conduction band is separated in energy from the Fermi level stabilization position more than the upper end of the valence band. In addition, as with the p-type doping described above, crystal defects that compensate for the doping are gradually introduced as the amount of doping increases. With n-type doping, there is no passivation because of H atoms, and carrier compensation because of self-forming lattice defects such as Ga vacancies and atoms in interstitial positions is typical. The diffusion rate for these lattice defects in the crystal is extremely high and they diffuse within the crystal during crystal growth from the sub-collector layer onward, penetrating the collector layer and reaching the base layer and emitter layer, which largely control the transistor characteristics. When the sub-collector layer is excessively doped, it causes a phenomenon where the transistor current gain is reduced. Therefore, it is important to use a doping concentration of an extent that does not introduce crystal defects (an example of the data is shown in **Fig. 5**).[9] However, the introduction of crystal defects is largely dependent on the crystal growth conditions, in other words, the maximum carrier concentration value can be increased by stoichiometric control. Moreover, technology for crystal defect control in this sub-collector layer and increasing carrier concentration can be applied in a similar manner for the sub-emitter layer formed from an n-GaAs layer that is positioned below the emitter contact layer and performs the role of linking electron transport between the InGaP emitter layer and the emitter contact layer.

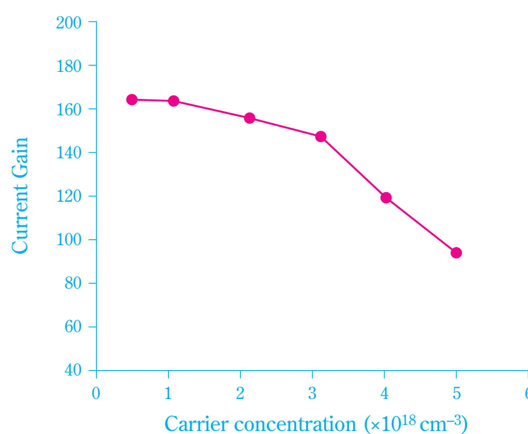

Fig. 5 Impact of sub-collector carrier concentration on current gain

3. Application in InGaP crystal growth and emitter layer

As described above, an emitter layer formed from a material with a larger band gap than that of the base layer is used to prevent the base current from leaking to the emitter in HBT. Either AlGaAs or InGaP can be used as the emitter material in GaAs lattice-matched HBT, and it is possible to have better performance by using InGaP because it can prevent hole current loss with a large energy barrier at the valence band, while reducing electron injection resistance at the conduction band edge between the emitter and the base. In

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addition, since AlGaAs crystals include chemically active Al, the density of the defects at the surface of the crystal exposed to the environment during device processing easily becomes high, and these defects at the surface form an electron or hole trap by which the device characteristics and reliability are affected. Because of this, it can be said to be more beneficial to use InGaP than AlGaAs, but there are also distinctive problems in terms of crystal growth in InGaP crystals. One of them is interface control. In MOCVD growth of crystal systems using As and P as group V atoms, the dissociation pressure for the group V atoms is high at the crystal growth surface, and group V material is typically supplied at a rate of several tens to several hundred times that of the group Ⅲ material. Crystal growth is carried out at supply rate limiting conditions for the group Ⅲ material. Therefore, group Ⅲ element switching is comparatively easy, and a steep hetero interface can be formed in heterojunctions with different group Ⅲ atoms. On the other hand, control of heterojunctions with different group V atoms is difficult. Since the group V atom dissociation pressure is high as described previously, the group V material supply must also be interrupted to suppress desorption of group V atoms from the crystal surface while interrupting growth at the MOCVD crystal growth surface for group Ⅲ–V compound semiconductors. During the formation of hetero interfaces with different group V elements, there is switching of this group V material, but cases occur in which substitution of the group V atoms on the crystal surface arises because of the magnitude of the dissociation pressure for the group V atoms at the crystal surface and the gas phase group V gas pressure. Therefore, the steepness of the hetero interface formed by the gas switching sequence at the heterojunction interface is affected. Specifically, for example, when InGaP crystal is formed on GaAs crystal, switching from the As material to the P material is carried out, but after the switching to the P material has been carried out, substitutions between the As atoms and the P atoms arise at the crystal surface because of the time elapsed before supply starts of the group Ⅲ material, in other words Ga material and In material, and crystals such as GaAsP may be formed. This is the degradation of the steepness of the heterojunction interface in a so-called interface transition layer and is a cause of a deterioration in device characteristics. To suppress this phenomenon, optimization of designs for MOCVD gas supply systems and gas switching conditions suitable for those systems is necessary.

The second problem in using InGaP crystals is the formation of a natural superlattice. In InGaP crystals formed by MOCVD growth, it is known that the lattice energy can be lowered with a lattice structure by regularly altering the In-rich group-Ⅲ sub-lattice plane and the Ga-rich sub-lattice and this phenomenon is the so-called natural superlattice formation.[10]

The formation of a regular arrangement of such altered sub-lattices in the <110> direction with InGaP crystal growth on a (100) crystal surface has been confirmed by x-ray diffraction (**Fig. 6**). It is known that if a natural superlattice is formed, distortion arises because of the difference in the bonding state of Ga atoms and In atoms with P atoms and in the lattice constant, and then a local polarization arises due to the change of charge balance induced by the distortion. This charging annihilates itself between adjacent sub-lattice planes inside the InGaP crystal, but a charge remains at the upper and lower interfaces for the InGaP layer as a whole. The amount of charge varies

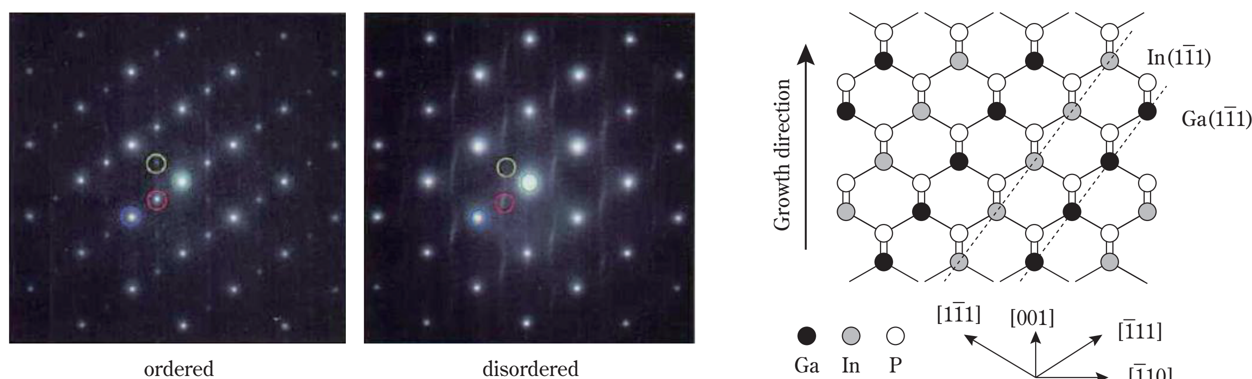

Fig. 6 Natural superlattice formation
(electron beam diffraction pattern difference - order/disorder)

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with the degree of formation of the natural superlattice, and that degree of formation depends on the growth conditions. In addition, it is known that the InGaP layer band gap value varies according to the degree of formation of the natural superlattice. Specifically, the greater the degree of formation of the natural superlattice is, the smaller the band gap becomes, and the reduction of the band gap at this time is thought to mainly arise on the conduction band side. This means that, while the energy barrier against hole injection from the base layer to the emitter layer is maintained on the valence band side, the energy barrier against electron injection from the emitter to the base gets smaller, so it is an advantageous direction for HBT operation. However, if HBT is fabricated using an InGaP layer with interface charging induced by a natural superlattice present in the upper and lower interfaces of this layer, the device characteristics are affected by the interface charging. In InGaP crystal growth on GaAs (100) crystals, a positive charge and free electrons are generated at the lower interface of the InGaP crystal because of the polarity induced, and a negative charge and free holes are generated at the upper interface. With the HBT structure shown in **Fig. 1**, a p-type base layer doped with high carrier concentration is present on the lower side of the InGaP emitter; therefore, the positive interface charging generated by the natural superlattice is canceled out by negative charging because of ionization acceptors in the base layer. When an n-type doped layer with high carrier concentration is present at the upper interface of the InGaP crystal, a similar interface charging cancellation is possible, but there are also cases of n-type layers doped with low carrier concentration because of HBT design. In such cases, the band of the InGaP layer is raised by the negative charge of the interface on the InGaP upper side interface, and this effect extends to the base/emitter interface (**Fig. 7**). **Fig. 8** shows a Gummel plot in that instance. When an interfacial charge is present, it is shown that the base current (I_B) increases in the low-voltage range, and as a result, the current gain decreases in the low current range. This is thought to be caused by the hole barrier at the base/emitter interface being lowered by the raising of the band at the upper-side InGaP crystal interface and hole injection to the emitter layer from the base layer increasing. Compensating for the charge on the upper side of the InGaP crystal can eliminate this effect. Specifically, n-type doping can be carried out in the vicinity of the upper side interface of the InGaP crystal, and the increase in the base current in the low-voltage range as shown in **Fig. 8** can be suppressed by using this method.[11)]

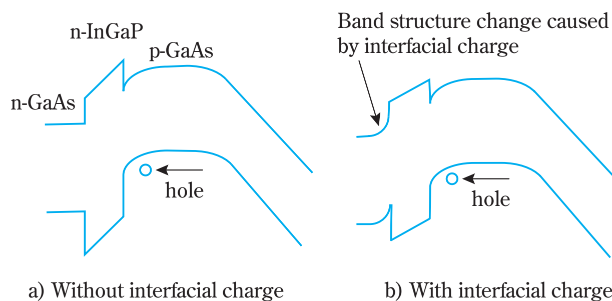

Fig. 7 Band structure change caused by interfacial charge between InGaP and GaAs

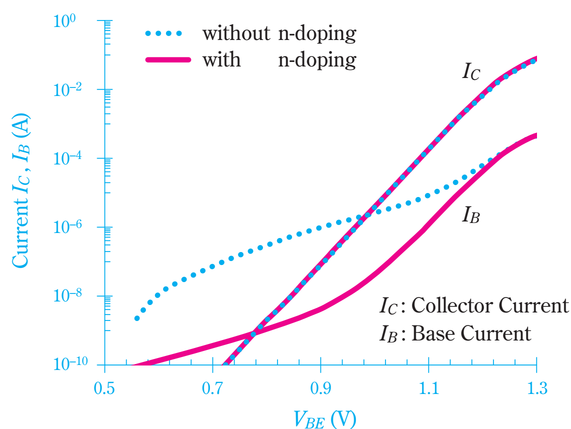

Fig. 8 Effect of InGaP interfacial charge on HBT Gummel plot

Problems for Making HBT Practical

While the basic performance of HBT devices using the technology described above satisfying practical standards has been achieved, problems arise in manufacturing the epitaxial substrates and in operating conditions. In the following, examples of these will be introduced.

1. Crystal defects in bulk GaAs substrates

As has been discussed up to this point, current gain and some other characteristics of HBT deteriorate by increase of recombination centers originated from crystal defects, impurities, etc. We have described the defects introduced by growth conditions, doping and other processes during epitaxial growth, but defects propagated from bulk GaAs substrates are also a cause

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of effects. Vertical gradient freeze (VGF), vertical boat (VB) and liquid encapsulated Czochralski (LEC) are manufacturing methods for GaAs substrates. Basically these methods are a kind of melt growth method, and crystals are grown near the melting point of GaAs, but at such high temperatures, the concentration of various types of point defects such as vacancies and interstitial atoms increases due to thermodynamic reasons. The point defect density or dislocation density can be also seriously affected by the manufacturing technique and the growth conditions through the fluctuation of stoichiometry and/or residual stress during crystal formation. Dislocation in the substrate is usually evaluated by the etch pit technique, and the substrates with dislocation densities around the $1 \times 10^3 cm^{-2}$ can be typically grown with VGF and VB, and ones with around $1 \times 10^4 cm^{-2}$ with LEC. Since these dislocations are in themselves active as recombination centers, they can be thought of as having large effects on HBT characteristics and reliability when they are propagated to the active area of HBT. There is also variation in the dislocation density itself, and that variation is a cause of variations in HBT characteristics, but the dislocations in themselves are also used as sources of absorption or release of various types of point defects as described above, and the behavior of dislocations and the various types of point defects are typically complex. In addition, some of these defects, as with the defects during high concentration doping of sub-collectors described previously, can be thought of as propagating to the active area of HBT and affecting important characteristics such as the current gain, etc. One measure for preventing these effects is introducing a layer that can block dislocation into the epitaxial layer. A typical dislocation propagation blocking method carried out with epitaxy in optical applications such as lasers is the method of multiple layer stacking of a pair of layers with different lattice constants (strained superlattice), bending dislocations in the interface direction using that strain energy and elimination to the outside of the crystal. In addition, another possible method, an impurity doping technique, has also been proposed to eliminate the dislocation to reduce the effects of dislocations on HBT characteristics.

2. Thermal runaway problem in HBT

In HBT, reverse injection current to the emitter from the base can be suppressed by a heterobarrier formed at the base-emitter interface; therefore, the base can be doped at a high concentration, and base resistance that limits high-speed operation can be reduced. However, during high density current drive, the current density in the peripheral parts of the emitter near the base electrode increases because of the effect of horizontal resistance in the base, and a current density difference with the center part where the resistance becomes large arises. To avoid the effects of this lack of uniformity, a design for forming an arrangement of multiple small electrodes is normally employed for the emitter. Therefore, the reduction of contact resistance with the electrode in emitters or of resistance in the emitter crystal layer is an important problem as was indicated earlier.

However the troublesome problem, so-called thermal runaway, is typically present in bipolar transistors, including HBT.[12] The thermal runaway mechanism is extremely simple. When a forward bias is applied across the emitter and the base, the current flowing from the emitter to the collector increases exponentially, and generates heat due to resistance along the current pathway. In parts where the amount of heat generated is large, the band gap of the semiconductor crystal is made smaller by the increase in temperature; therefore, the energy barrier for injection current from the emitter is reduced, and the current density increases further. Typically current density differences arise between emitters or even within an emitter forming HBT because of some variation in size of each emitter due to limited processing capability among the multiple emitters or differences in distance from the base electrode even within the same emitter (resistance differences), and further, because of natural fluctuations when multiple emitters are present in parallel. Once current density differences arise, a positive feedback action that concentrates current further in parts with high current density because of temperature differences that occur there arises, and finally, crystal breakdown arises because of the electric field caused by abnormal current density or thermal effects.

This is the so-called thermal runaway phenomenon. To suppress this phenomenon, countermeasures such as positioning of emitter electrodes or making temperature uniform by heat exchange through wiring connecting those emitters and improvements in heat dissipation are employed. When the temperature increases in homo bipolar transistors or AlGaAs/GaAs HBT where the valence band barrier is comparatively small, the base current flows out to the emitter side to

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a certain extent; the base potential rises, and there is a negative feedback action that reduces the current injection from the emitter, while InGaP/GaAs HBT, etc., that have large valence band barriers, are especially vulnerable to thermal runaway even though they have superior temperature characteristics. Thus, mechanisms are used for suppressing current concentration by forming a so-called ballast resistance, which has thermistor characteristics of resistance increasing during increases in temperatures in emitter electrode parts, and automatically increasing resistance in parts where temperature increases have arisen. This ballast resistance is commonly formed on top of emitter electrode parts, but it is also frequently formed within semiconductor crystal layers. Most semiconductors normally have negative temperature characteristics, and it is possible to have a function as a ballast layer by achieving comparatively large negative temperature characteristics. However, these ballast layers cause loss just as resistance in the typical operating conditions for transistors does; therefore, the development of an HBT crystal structure having lower resistance and an effective thermal runaway suppressing function is one challenge for the future.

HBT Device Simulation

To design HBT having the targeted electrical characteristics, three major parameters; the layer thickness, composition (Al ratio in AlGaAs, etc.) and impurity concentrations (Si, C and other impurity concentrations) must be optimized for each layer. HBT requires many processes, much time and effort for device formation, including microprocessing at a practical level, but on the other hand, HBT which has a large emitter area of around 100 μm requires no special microprocessing, and devices can be formed with a time of approximately three hours at the shortest using simple processing technology. This large emitter device is naturally different from a commercial product device, but several important device parameters, including current gain in low current density regions, can be extracted in a short cycle time, and the technique is extremely useful from the standpoint of epitaxial crystal development for HBT and quality assurance for products, so it is widely used. However, when we simply think of the design of three layers for the emitter, base and collector constituting HBT, even if there are two levels for each of the three major parameters above for the three layers, their total number of combinations is $2^{3\times3}=512$, and conducting an experiment for all of them is not realistic if we consider the limited development period and costs. Furthermore, the three layers above are divided more finely into the emitter contact layer, sub-emitter layer, ballast layer, sub-collector layer, interface layer etc., and, further, the parameters to be optimized and the levels to be studied for them make for an astronomical number. Sumitomo Chemical had already developed a device simulator for epitaxial wafers for p-HEMT, and to address this problem, we made use of that development and created an HBT device simulator for handling HBT development. An overview of that technology is described in the following.

The HBT simulator we created is based on the drift diffusion method.[13] The drift diffusion method is a method that expresses the current by the sum of the drift current dependent on electric field strength and the diffusion current dependent on the gradient of the carrier (electrons or holes) concentration, but it is a rough approximation of the Boltzmann transport equation (Wigner transport equation when considering quantum mechanics). Therefore, the calculation speed of the drift diffusion method is more rapid than that of the hydrodynamic method or the Monte-Carlo method, with less approximation, but the difference between the calculated and measured electrical characteristics is large. To make this difference smaller, we referred to multiple HBT current-voltage characteristics measured by Sumitomo Chemical, and we adjusted the physical parameters such as electron and hole mobility, as well as band offset energy at different types of compound semiconductor interfaces (hetero interfaces). (Naturally, when a technique with less approximation is used sacrificing calculation speed, these physical parameters take values closer to those measured.) Another area in which ingenuity was used was the calculation method for current in the vicinity of hetero interfaces. In a typical semiconductor device simulator, the thermionic-field emission boundary condition (specifically, boundary conditions calculating the interface current with the idea of "using the thermal energy and tunnel effect when the carrier overcomes the energy barrier at the hetero interface") is set only at the hetero interfaces.[13] We proposed a method for setting values for the carrier current density in the vertical direction to hetero interfaces by taking the weighted average of the carrier current density calculated based on the drift diffusion equation and that calculated based

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on the thermionic-field emission boundary condition in the vicinity of hetero interfaces.[14)]

In this method, the drift diffusion current is the main one at a point a certain distance away from the hetero interface, but as the hetero interface is approached, the ratio of the thermionic-field emission boundary condition current to the drift diffusion current increases, and at the hetero interface, only the thermionic-field emission boundary condition current is used. If current-voltage characteristics are calculated by this method, the difference between the calculated and measured current-voltage characteristics is smaller than when the thermionic-field emission boundary condition is only set at the hetero interface.[14)] An example of the current-voltage characteristics (Gummel plot) calculated using the HBT simulator described above is shown in **Fig. 9**. The calculated results agree well with experimental results. Currently, at Sumitomo Chemical, the HBT simulator described above is fully utilized for designing and optimizing the epitaxial layer structure, with numerical predictions of HBT Gummel plots, current gain, collector-base voltage resistance, emitter-base voltage resistance, elucidation and suppression of the thermal runaway phenomenon, etc.

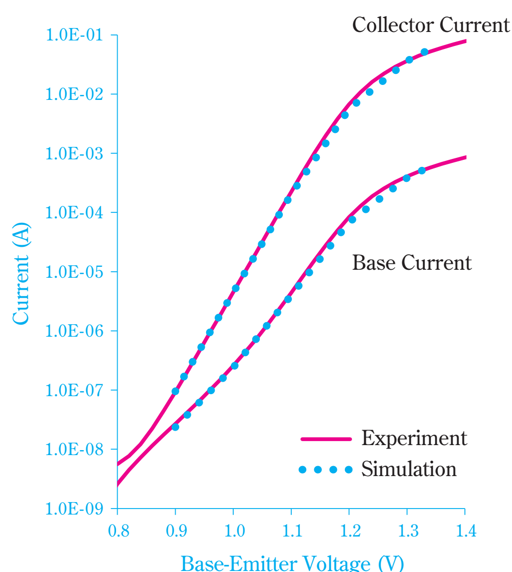

Fig. 9 Gummel plot comparison between simulation and experimental results

Conclusion

Based on the technology described up to this point, Sumitomo Chemical has manufactured and sold HBT epitaxial wafers for power amplifiers targeting mobile communications. Recently, a BiHEMT structure where HBT power amplifiers, low noise amplifiers and switches formed by p-HEMT can be integrated has also come into use; increased complexity and greater functionality in the structures of epitaxial substrates have been progressing, and quality, which is required from the standpoint of manufacturing, has also been increasing. To achieve these things, we must continue to make progress in strengthening development functions and improving manufacturing technology. Compound semiconductor materials are more replete with variety in terms of material design and control of characteristics than Si, and there are expectations for further expansion of devices that can make use of compound semiconductors. The factors that determine the performance limits of equipment related to electronic information, which is becoming more complex and more various, can be said to be in a large part the characteristics of the semiconductor materials themselves. At Sumitomo Chemical, we are making the utmost use of crystal growth and analysis evaluation technology, and we would like to continue to hold up our end of the expansion of the compound semiconductor market.

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