Present Status and Future Prospect on ULSIs and Related Semiconductor Materials

Sumitomo Chemical Co., Ltd.
Advanced Materials Research Laboratory
Masahiko HATA
The University of Tokyo
Department of Electrical Engineering
Graduate School of Engineering
Shinichi TAKAGI
Mitsuru TAKENAKA
National Institute of Advanced Industrial Science and Technology
Nanoelectronics Research Institute
Tetsuji YASUDA

The performance of ULSIs (Ultra Large Scale Integrated Circuits) has been dramatically enhanced over 30 years by increasing the number of transistors per unit area and the operation speed per single gate simultaneously by the miniaturization technology through the guiding principle of the scaling rule applied to Si CMOSFETs (Complementary Metal-Oxide-Semiconductor Field Effect Transistors). However, miniaturization of the transistors becomes increasingly difficult due to physical limitations, and the conventional scaling rule will not be enough to enhance the performance of the ULSIs. Thus introducing new device structure, new processes, and new materials become increasingly important. The present status of and future prospects for new semiconductor materials for next generation ULSIs are reviewed in this paper.

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Future Prospects for LSI Development

1. Improvements in transistor speed and integration through CMOS technology and miniaturization

Up until now, the developments in ultra-large-scale integrated circuits (ULSIs) have basically been supported by greater integration and higher performance in metal-oxide-semiconductor field effect transistors (MOSFETs) through the use of scaling rules. Here, a scaling rule means a device design rule for miniaturization that reduces all of the parameters related to the shapes of devices by the same proportion, and along with this, voltage values are reduced proportionally in a similar manner. As a result of intently pursuing miniaturization by basically following these rules from the 1960s to now, dies that integrate several hundred million very tiny transistors with MOSFET channel lengths around 30 nm where the closest proximity for gate pitches between adjacent MOSFETs is around 120 nm have currently become practical.

Fig. 1 is a prediction of future development trends in logic LSI technology published by IBM.[1)] Next year, mass production will begin using technology known as the 22 nm technology node in which device pitches are 80–100 nm. Following this, a new generation having miniaturized device pitches and channel lengths will move into mass production every two to three years, and in the 2020s, we are expecting to

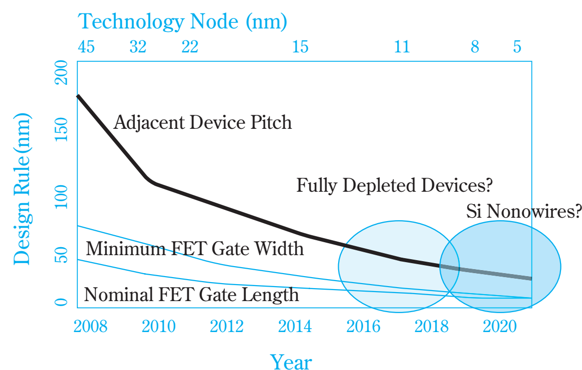

Fig. 1 Scaling trends for design rules for ULSIs [Data from reference 1)]

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move into the nano-CMOS (complementary MOS, complementary type MOSFET) era with gate lengths of 10 nm or less.

The miniaturization of CMOS according to these scaling rules had basically been able to satisfy two requirements simultaneously up to the year 2000: (1) increases in the number of devices per unit area/ increased circuit scale and (2) increases in performance through improvements in response speed for each stage of the devices. Therefore, scaling has provided the greatest and strongest guiding principle for sources of additive value in dies.

2. MOSFET power consumption, ON-state current and short-channel effects

Here we will briefly touch upon the three elements, power consumption, ON-state current (MOSFET drive current) and control of short-channel effects, which affect the performance that must be achieved in MOSFETs as devices used in LSIs. First of all, the reduction in power consumption is currently the most important problem for future logic LSIs.

Up to now, reduction in power consumption has been of the greatest interest in the realization of integrated circuits. **Fig. 2** shows the changes in power consumption by LSIs by decade.[2)] To reduce the power consumption of logic LSIs formed using the bipolar transistors that were used in the beginning, n Channel MOSFET resistive load logic was introduced. Thereafter, the problem of increases in power consumption was solved by introducing CMOS, with which the leak current during standby can be made sufficiently low. However, if we limit our discussion to CMOS, in the simplest terms, the power consumption is fixed per unit area by the scaling rule; therefore, reductions in power consumption cannot be achieved. In addition, the actual power supply voltage for a die cannot be reduced like the scaling rules; therefore, the power consumption per chip when operating continues to increase. Additionally, in recent years, the leak current in MOSFETs has been increasing with each generation due to a variety of causes that will be discussed in the following, and standby state power consumption rather than that during operation is predominant. Therefore, reduction of the leak current when the CMOS is off is an urgent problem.

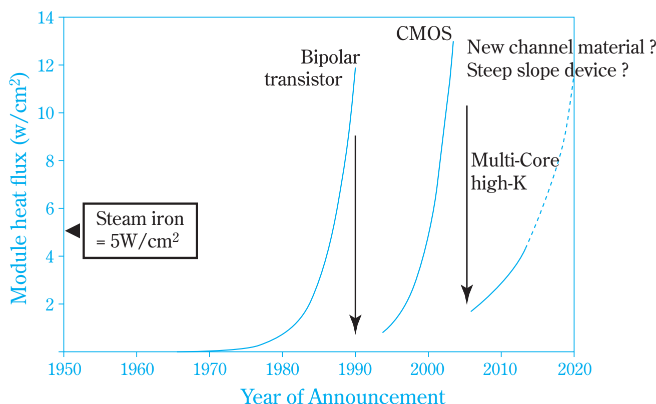

Fig. 2 Power consumption in integrated circuits

Next, the ON-state current (MOSFET drive current) is also an extremely important index of performance in logic LSIs for which improvements in computation speed are indispensable. MOSFET operating speed is basically determined by the charging or discharging time for the next stage gate capacitance going from the power supply voltage to the ground voltage or vice versa. The next stage gate capacitance includes the interconnection capacitance and a variety of parasitic capacitances that cannot be scaled; therefore, to increase the operating speed and increase the clock frequency, the drain current value at the power supply voltage must be increased per unit channel width.

In addition, a requirement for LSI devices is being able to fabricate the extremely large number of several hundred million MOSFETs with characteristics according to the design and without variations. Therefore, the short-channel effects must be controlled. Short-channel effects are generally a phenomenon in which the channel length is made smaller and the controlling force for the channel current for the gate voltage is reduced by applying a drain voltage, thus reducing the threshold voltage. In terms of device fabrication, a certain degree of variation in the MOSFET channel length, which is formed by lithography, cannot be avoided; therefore, if the short-channel effects are large, the variations in the threshold voltage and drain current among devices increases, and circuit operation becomes impossible. Therefore, it is necessary to increase the influence of the gate voltage on the channel electrons and control the short-channel effects.

3. Limiting factors hampering scaling rules

However, after the 90 nm technology node, it has become difficult to improve performance just by miniaturization according to scaling rules because of a variety of physical limitations. This is because there is a trade-off relationship among the three elements neces-

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sary as described earlier for achieving MOSFETs, ON-state current, power consumption and control of short-channel effects; in terms of miniaturization, and with miniaturization alone, the required specifications for these three elements are no longer satisfied.

This situation is shown schematically in **Fig. 3**.[3] For example, when scaling rules are followed, gate insulating layers must be made thinner. This is because, with the same gate voltage, there will be a high ON-state current, and the influence of the gate voltage on the channel electrons will increase. This is effective for controlling the short-channel effects. However, at the 65 nm technology node, the gate insulating layer thickness has become extremely thin at around 1.5 nm, and making the gate insulating layers thinner causes an increase in rapid leak current and power consumption because of tunnel current between the channel and the gate. In addition, the concentration of impurities in the substrate must be increased for scaling the width of the depletion layer for CMOS on a bulk Si substrate to control short-channel effects. However, increasing the concentration of impurities in the substrate reduces the mobility of channel electrons and holes and reduces the ON-state current by increasing the impurity scattering and increasing the effective electric field. In addition, increases in junction leaks and increases in power consumption are induced. Furthermore, shallower source and drain junctions are necessary to control the short-channel effects. However, if the junctions are made shallower without sufficiently increasing the concentration of impurities for the source and drain, the resistance in the source-drain area will increase and, as a result, will cause a reduction in ON-state current.

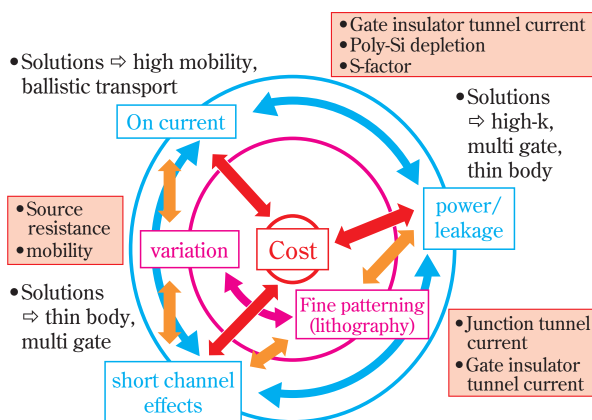

Fig. 3 Relationship among design factors for transistors

In addition, the inability to sufficiently reduce the MOSFET threshold value is an important problem. **Fig. 4** shows a schematic of the relationship between MOSFET gate voltage and drain current. At the threshold voltage (V_{th}) or less, the drain current decreases exponentially, but, as the figure shows, if the drain current is plotted as the log, it has a finite slope. The gate voltage, found as a quantity with the quantification of this slope, required to change the current by a factor of ten is called the S factor. Because of the operating principles of MOSFETs, the S factor cannot in principle be lower than 60 mV/dec, and if the short-channel effects worsen, this value will be even higher. As a result, if the OFF-state current at a zero gate voltage, which determines the current when the LSI chip is on standby, is set to a certain value, the lower limit for the threshold is determined from the S factor. Since this value cannot be reduced by scaling, it is in principle difficult to reduce the MOSFET power supply voltage by scaling.

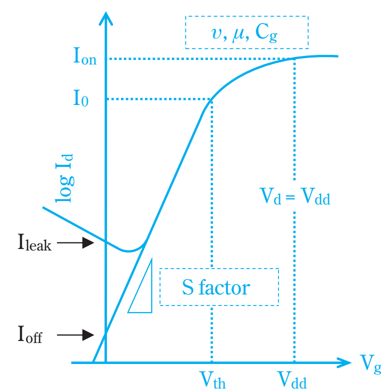

Fig. 4 Schematic of relationship between drain current and gate voltage in MOSFETs and definition of S factor

In addition to the trade-off between these values, the cause of limitations to miniaturization which has been forcefully viewed as a problem in recent years is variations in the characteristics of the devices. This is also affected by variations in processing during the fabrication of devices, but more fundamentally, the origin is statistical variations because of a reduction in the number of impurities in the channel with the miniaturization of MOSFET channels. Since it is necessary to set a threshold voltage and power supply voltage to take into account a margin for variations to make the circuit operate appropriately in consideration of variations in characteristics, an important factor currently hamper-

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ing voltage reductions in MOSFETs is this variation in MOSFET characteristics.

In addition, there is a technical problem in achieving lithography technology capable of fine processing down to the 10 nm level. Currently, extended UV (EUV) exposure technology is the most powerful candidate, but the maturity of the technology is still lower than photolithography using ArF excimer lasers that has been used for the finest processing conventionally. Furthermore, when we consider LSIs as products, cost is an important point in terms of practical constraints. Increases in the difficulty of the technology and complexity of production processes eventually increase costs even if they are technically solvable.

Technology Booster Techniques

1. MOSFETs using new structures and new materials

Since the trade-off relationship shown in **Fig. 3** and the variations in MOSFET characteristics due to the statistical variations in impurities are determined by the fundamental physical mechanisms, the problems are not solved for MOSFETs on conventional bulk Si substrates even if the impurity concentration and oxide film thicknesses are optimized. Therefore, starting in the year 2000 (90 nm technology node era), we decided to pursue a method for achieving new devices while resolving the trade-off relationship problems by introducing new technology that would improve the characteristics for MOSFET power consumption, ON-state current and short-channel effects in addition to scaling. This technology for improving the performance of the various devices is called a technology booster, and the method for moving forward with miniaturization using this procedure is called equivalent scaling. A typical technology booster is a strained Si, high-k/metal gate-gate stack, and multi-gate structure. A characteristic of this technology is that the MOSFET structure becomes complicated, and new materials that have not been used in conventional Si technology are introduced. It is not too much to say that logic LSI development from the 90 nm technology node onward has moved forward through a process of clarifying which generation these new technology boosters will be introduced in.

Fig. 5 shows an outline of the future device technology trends described in the ITRS 2010[4] International Technology Roadmap for Semiconductors. Starting in 2011, it is predicted that micro MOSFET development will sequentially introduce thin-film body structures which will be discussed in the following, multi-gate structures, group Ⅲ-V compound semiconductor/Ge channel structures, etc. It is easily seen from this figure that it is indispensable to continuously introduce new technology booster techniques with the introduction of new structures and new materials that have been moving forward continuously since 2000. The following gives a brief introduction to several of these technology booster techniques.

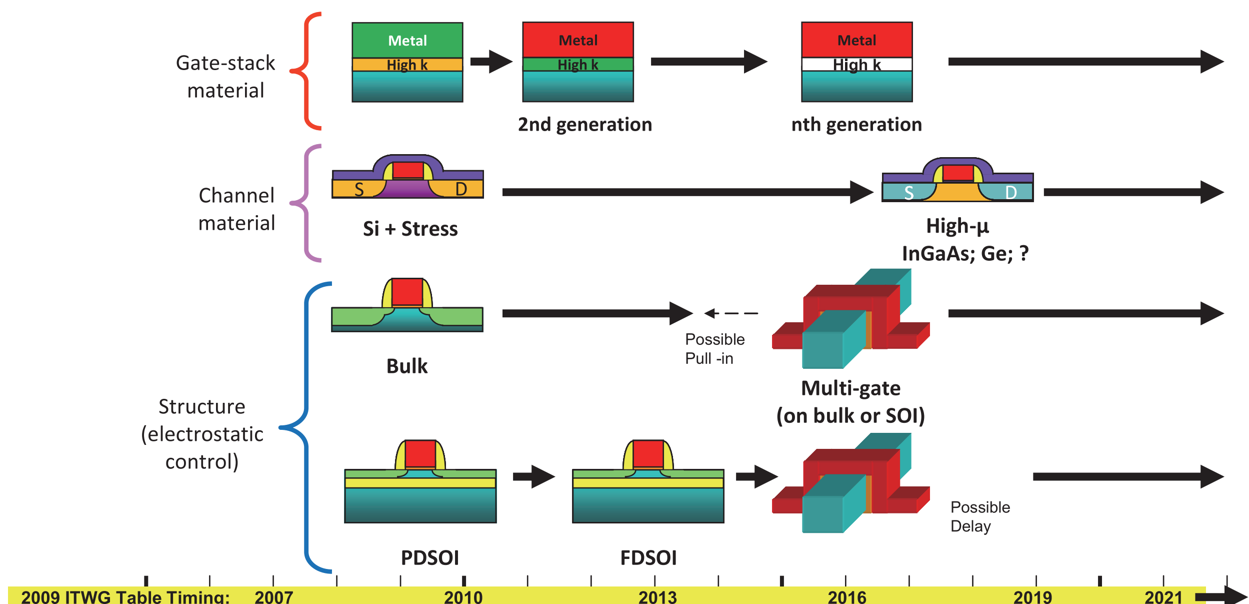

Fig. 5 Technology roadmap for MOSFET device structures[4]

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2. High-k/metal gate-gate stack structure

Increasing the gate oxide layer capacitance, that is making the oxide layers thinner is useful for many aspects of MOSFET characteristics, such as improving short-channel effects, ON-state current, low voltage operation and S factor as well as controlling the threshold value variations. However, increases in gate current because of tunneling as a side effect of making the layers thinner is an important problem. Thus, by using a high-k insulating layer, which has a dielectric constant higher than the conventional SiO_2 without physically reducing the thickness of the oxide layer and by using metal electrodes instead of a gate made of polysilicon, which is a semiconductor even though it is doped at a very high concentration, a high-k/metal gate-gate stack structure capable of having a large gate capacity was developed without giving rise to parasitic capacitance due to depletion of the gate electrode itself. This is an extremely effective new material technique for MOSFET scaling, and Intel Corporation introduced[5] the 45 nm technology node using a hafnium-based material. This technology is essential for the future.

The problem with high-k insulating layers is that, if a direct interface is formed between the high-k insulating layer and Si, mobility decreases because of a deterioration in the interface characteristics. Currently, an extremely thin SiO_2 insulating layer is inserted as an interface layer to control drops in ON-state current, but with this layered structure, it is extremely difficult to achieve an equivalent insulating thickness that is even thinner as required by future generations of technology. Achieving high-k insulating layer/Si MOS interface layers with excellent characteristics and making further increases in the dielectric constant of high-k insulating films are necessary.

In addition, the problem of not being able to suitably control threshold values for both nMOSFETs and pMOSFETs because of the thermal instability of metal electrodes combined with high-k insulating films has not been sufficiently solved at present. Moving forward, we must select suitable material systems and processes in the technology for further integration.

3. Thin film body structures and multi-gate structures

To control short-channel effects, the influence of the gate voltage on the channel electrons arising in the MOS interface must be increased. To this purpose, it is effective to make the channel layer an extremely thin film (thin-film body structure) as in thin-film Si-On-Insulator (SOI) devices and, further, to form the gate electrodes around this thin-film body (multi-gate structure). Because of the above, we can assume that the channel structures will progress in order from single gate FETs on thin-film SOI to double gated dual-fin-FETs, triple gated tri-gate finFETs and finally nanowire FETs in which the gate electrode is wrapped around the channel like a wire, as is shown[6] schematically in **Fig. 6**. Very recently, Intel Corporation made it clear that finFETs would be used in MOSFETs for the 22 nm technology node, and we have come to the era when thin-film body structured multi-gate structures will finally be achieved.

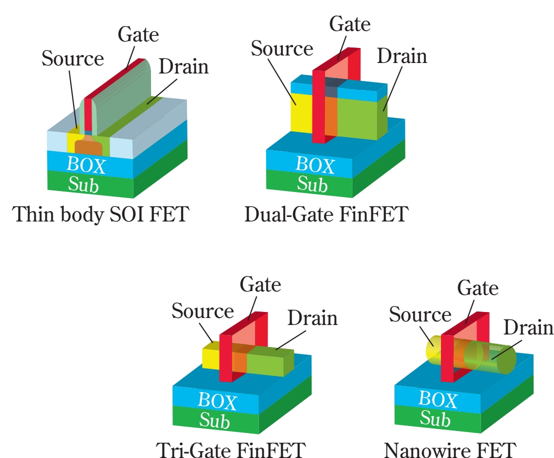

Fig. 6 Expected changes in MOSFET gate and channel structures

With this device structure, the short-channel effects can be controlled, not by the electric field formed by substrate impurities, but by the effects of the shape of the physical structure. An intrinsic channel that contains no impurities can be used for the channel, and the variations in threshold value and variations in characteristics due to the variations in impurities can be reduced by controlling the threshold value using the gate electrode. On the other hand, there are problems with the highly precise processing technology for forming three-dimensional MOSFET structures, reducing parasitic resistance and capacitance and achieving MOSFETs with different threshold values on the same substrate.

4. Strained Si technology

If a large stress is applied to Si, its electronic band structure is modified. Therefore, by adding strain to

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the Si channel by using suitable stress, the effective mass of electrons is reduced or the density of electron carriers with lighter effective mass is increased, thus improvements in channel mobility and an increase in current drive force are possible.[7] Using this method, strained Si technology, which achieves improvements in MOSFET ON-state current, is being actively used in CMOS for the 90 nm technology node[8] onward. The introduction of strain into the channel is done by including materials that have locally strong stress, and in a variety of techniques for introducing strain have been developed and made practical. **Fig. 7** schematically shows a typical method for introducing strain. nMOSFETs that have electron channels constituting the CMOS and pMOSFETs that have hole channels have different optimal strain orientations; therefore, innovations are being made in structures and processes to be able to introduce the optimal strain for each of them. Strained Si technology uses conventional Si as is for the channel material, and by getting used to using stress materials, such as SiGe and SiN, that are well known in Si technology, it is possible to effectively increase the MOSFET ON-state current without greatly sacrificing other electrical characteristics. Therefore, strained Si technology has rapidly developed during the last 10 years, and is recognized as technology that is indispensable for advanced CMOS logic. On the other hand, because the improvements to Si performance through strain have just about reached a point of saturation and the introduction of strain will be difficult with further progress in miniaturization, it is thought that ON-state current improvement technology that plays the role of post-strained Si, such as channel materials other than Si, such as Ge, graphene and group Ⅲ-V compound semiconductors, which will be discussed in detail in the following section, will become necessary.

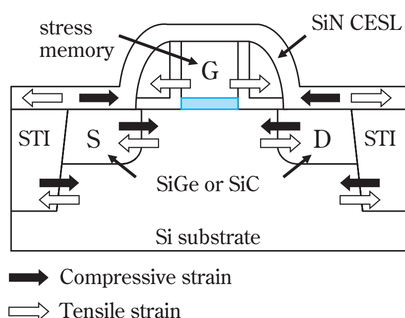

Fig. 7 Typical structure of MOSFET with local strain introduced

Compound Semiconductor MOSFET Technology

1. Basic characteristics of group III-V compound semiconductors and MOS interface problems

Group Ⅲ-V compound semiconductors are semiconductors formed from Al, Ga, In and other group Ⅲ elements that form trivalent cations and N, P, As, Sb and other group V elements that form trivalent anions. The main characteristics of Si and Ge, which are group IV semiconductors, are the ability to fabricate high speed, high frequency devices with electrons as carriers because of the large electron mobility and the suitability for applications in high efficiency, high sensitivity light emitting and receiving devices because electron transfer between the valence band and conduction band is direct without assistance from phonons. In addition, it is possible to continuously change the band gap and crystal lattice constant by forming alloys of multiple group Ⅲ-V compound semiconductors (AlN-GaN, AlAs-GaAs, GaAs-InAs, GaP-InP, etc.), and a variety of device designs are possible when these are used in heterostructures.

MOSFETs that use group Ⅲ-V compound semiconductors for which development is currently progressing make high-speed, high-frequency operation possible with the possibility of operation with low power consumption; therefore, there are expectations for applications in post-scaling generation CMOS and communications devices. The important physical properties for MOSFET applications for the main group Ⅲ-V compound semiconductors are given in **Table 1**. Semiconductors with a small electron effective mass have a low effective density of states in the conduction band, and can be seen as having a large electron mobility. In general, a large electron mobility is advantageous for making a large current flow with a lower fixed voltage. On the other hand, when the gate insulating layer thickness is scaled down to several nanometers or less in MOSFETs that use semiconductors with large mobility, the surface carrier concentration is inhibited because of a low effective density of states, and there is a possibility that the effect of increasing the ON-state current is canceled out by the increased mobility. The trade-off relationship between this mobility and density of states is a point that must be considered when selecting group Ⅲ-V compound semiconductors for MOSFET applications.

Another point that should be considered in relation-

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Table 1 Electronic characteristics of typical semiconductors

	Si	Ge	GaAs	InP	InGaAs(In 53%)	InAs	InSb
Electron mobility (cm^2/Vs)	1600	3900	9200	5400	12000	40000	77000
Effective Mass of electron, m_t/m_0	0.19	0.082	0.067	0.082	0.041	0.023	0.014
Hole mobility (cm^2/Vs)	430	1900	400	200	300	500	850
Bandgap (eV)	1.12	0.66	1.42	1.34	0.74	0.36	0.17
Effective DOS in conduction band (10^{19} cm^{-3})	2.8	1.04	0.047	0.057	0.021	0.0087	0.0042

ship to the physical properties of semiconductors is the fact that it is desirable for the band gap to be large for controlling the OFF-state current. In addition, the conduction band for semiconductors is generally constituted of multiple components having different electron effective masses, such as a Γ valley, an L valley and an X valley, and group Ⅲ-V compound semiconductors, starting with GaAs, have the most energy stable Γ valley that has the smallest electron effective mass among these. However, electron transfer from this Γ valley to a L valley, which has a large electron effective mass, arises with high surface carrier density or in a large electric field. The fact that it is preferable to have a large difference in energy between the valleys to avoid a reduction in mobility because of this transfer between the valleys is a point that should be considered. In addition to the various factors above, current MOSFET research on using group Ⅲ-V compound semiconductors is focusing on InxGa1-xAs, which is an alloy of InAs and GaAs because of the ease of controlling the MOS interface as will be described in the following. In most cases the x in the In composition is set to x = 0.53 so that the InxGa1-xAs epitaxial layer matches the lattice in an industrially produced InP wafer.

The basics of MOSFET operations are changing the position of the Fermi level for the semiconductor surface by applying a voltage to the gate electrode and increasing (ON-state) and lowering (OFF-state) the surface carrier concentration. To control the leak current flowing between the metal used for the electrode and the semiconductor surface, an insulating layer is inserted between the two and usually a dielectric material with a large band gap is typically used for this insulating layer. Oxide materials, which are particularly stable when operating in air, are generally used. Therefore, carriers are induced at the interface between the insulating oxide layer that is inserted and the semiconductor by an electric field applied to the metal electrode. This interface is generally known as a metal-oxide-semiconductor (MOS) interface, but compared with a Si MOS interface using Si as the semiconductor and SiO_2 as the insulating layer, a high interface state density typically arises in MOS interfaces (called group Ⅲ-V MOS interfaces in the following) that use group Ⅲ-V compound semiconductors. This causes what is known as a pinning phenomenon that prevents changes in the surface Fermi level, and as a result, it is extremely difficult to control the interface carriers due to the metal electrode, making MOSFET operation difficult. To solve this problem, oxide films were formed by various oxidation methods (thermal oxidation, anodic oxidation and plasma oxidation) and insulating film deposition methods (vapor deposition, sputtering, CVD and sol-gel) on GaAs and InP semiconductors, and attempts had been made to reduce the interface state density. However, this did not get to the point of establishing MOS interface forming technology with sufficient practical quality. Information on this area is summarized in “Physics and Chemistry of Ⅲ-V Compound Semiconductor Interfaces” (edited by C. W. Wilmsen, Plenum Press, New York, 1985).[9] In this book, based on the history of the confusion among researchers produced by an erroneous interpretation of C-V measurements by Meiners, it was stated that “we cannot believe there is accumulation and inversion at the Ⅲ-V interface until the operation of a normally-OFF MOSFET shows in both the p channel and n channel” to show without doubt that there was accumulation and inversion at the Ⅲ-V MOS interface.

Research and development on Ⅲ-V MOSFETs is difficult; therefore, the main trend is using Schottky gate FETs that form direct junctions between the gate metal and GaAs crystal layer a in FETs made with GaAs, which is a typical material for them. A high density interface (surface state) arises on the GaAs surface as described above and surface Fermi level pinning occurs, but because of this, a surface potential barrier (Schottky barrier) of a fixed value (approximately 0.8 eV) is formed regardless of the type and work function

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of the metal at the junction. This Schottky barrier is seen as a type of pseudo-insulating gate layer, and by modulating the gate potential through this layer, it is possible to modulate the conductive channel current formed inside the GaAs, making operation as a FET possible. High density current operation is difficult in interface accumulation or inversion mode, which require a large voltage amplitude, because the Schottky barrier layer potential barrier is smaller than the oxide film gate layer used in MOSFETs, but high-speed operation is possible taking advantage of the GaAs electron mobility which is much greater than that of Si. In particular, in high electron mobility transistors (HEMT) which were invented by Mimura, Hiyamizu, et al. from Fujitsu Ltd. in 1978,[10] the use of the metal and Schottky barrier are the same, but an AlGaAs layer, which has a comparatively larger band gap, is used for the gate layer, and GaAs is used for the channel layer. In addition, a so-called modulation-doped structure in which the doping impurities, which are necessary for adjusting the channel electron density and FET threshold value, are only doped on the AlGaAs layer side is used. In this structure, the channel electrons are induced on the GaAs side at the AlGaAs·GaAs interface, but ionized doping impurities, which are an important factor in scattering electrons are only confined on the AlGaAs side in the neighborhood of room temperature; therefore, there is a great improvement in the mobility of the electrons flowing in the channel. The advantages of high electron mobility, which is a characteristic of group Ⅲ-V compound semiconductors, can be brought out to their maximum limits. Therefore, development and practical realization of group Ⅲ-V compound semiconductor FETs thereafter shifted to this HEMT system.

2. Development of HEMT technology and applications in high-frequency devices

From the latter half of the 1980s and past the 1990s, there was more progress in improving the HEMTs described above, and pseudomorphic HEMTs (p-HEMTs), in which the channel layer was replaced by an InGaAs quantum well layer, which has superior electron transport properties and higher electron mobility, were developed. These p-HEMTs are commonly used in front end modules (low noise amplifiers (LNA) that receive and amplify high-frequency signals; high efficiency power amplifiers (PA) for amplifying and transmitting signals from terminals and low loss switches (SW) for high-speed switching of this receiving and transmitting) in the ultrahigh frequency band of 1 to several tens of GHz commonly used in various wireless communications of which mobile telephones are currently the main focus. Here, we will briefly touch upon switch (SW) applications which have an intimate relationship with MOSFETs for the digital integrated circuits that we have been discussing from the beginning in terms of their operating mechanisms and performance factors.

In p-HEMTs, the maximum value for the drain current is related to the maximum power that can be handled by the switch along with the voltage the gate can withstand. On the other hand, the minimum value is the leak current during OFF-state operation, and reduction (increasing OFF resistance) of this leak current is important for assuring isolation from a signal traveling in a circuit path when one circuit path is in the ON state in switch operation and another circuit path in the OFF state. In addition, when high frequency signals are handled in the OFF state, a loss arises through the residual capacitance during the OFF state. In terms of this high frequency loss, the fact that the parasitic capacitance component arising with the use of substrates like Si, for which increasing the resistance is difficult, in GaAs switches that make use of high resistance semi-insulating substrates is small enough to be ignored is an important advantage of GaAs switches, as has been discussed already. **Fig. 8** shows the typical current-voltage characteristics for FETs. The reciprocal of the drain current rise (slope) in the linear area for low drain voltage is defined as the ON resistance (R_{on}). This R_{on} has an intimate relationship with the insertion loss during ON operation and is an index directly connected to the noise factor for a LNA when receiving high frequency signals or the effective efficiency of a PA during transmission.

The p-HEMT R_{on} can be roughly divided into two components, i) transverse channel resistance in the InGaAs quantum well forming the channel and ii) vertical resistance from the ohmic electrode injection part to the channel. R_{on} is substantially expressed by

$$R_{on} \propto L_g / (\mu_n \cdot C_i \cdot Z)$$

and with conditions of the same gate dimensions ($L_g \times Z$), gate capacitance (C_i) is inversely proportional to electron mobility (μ_n). For a p-HEMT or MOSFET, C_i is proportional to the two-dimensional electron density induced in the channel layer, and the higher this is, the more effective it is for R_{on}, but as a result of

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At Linear Region, I_{ds} can be described;

$$I_{ds} = \frac{Z}{L_g} \mu_n C_i (V_g - V_{th}) \cdot V_{ds}$$

L_g : Gate length　Z : Gate width
μ_n : Electron mobility
C_i : Gate capacitance
V_g : Gate voltage　V_{th} : Threshold voltage

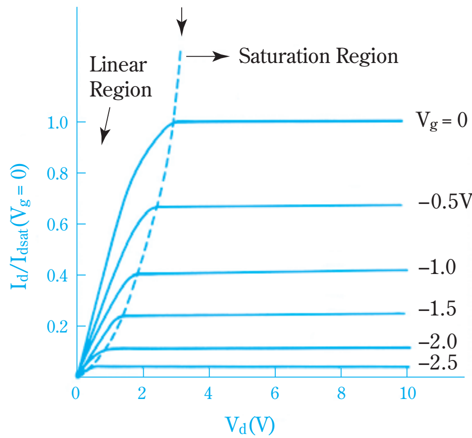

Fig. 8 Schematic of I-V characteristics in FETs

increases in the gate charging and discharging capacitance that accompany ON and OFF, it induces an increase in power consumption. The point is that the capacitance can be controlled by miniaturizing the gate length (L_g) itself, but more advanced microprocessing technology is necessary, and with HEMTs that use Schottky gates, there is a constraint that the gate layer itself cannot be made too thin (C_i cannot be made large) because of the need to maintain gate voltage resistance. Therefore, InGaAs, which has an even higher mobility than GaAs and of course Si, is used in the channel because of these points of having no trade-off with other characteristics and having the most desirable electron mobility increase. Along with this, AlGaAs, which has a large band gap and is comparatively effective for large voltage resistances, is used for the gate layer in combination with the InGaAs channel to construct a rational p-HEMT structure.

InGaAs channel p-HEMT switches are widely used as high-frequency switches, but reductions in R_{on}, which are a problem with high-frequency switches, are also a problem which is common to improvements in the drive current necessary for improving operating speed in integrated circuits as described in sections 1 and 2. Group Ⅲ-V compound semiconductors, which have high electron mobility, also have superior intrinsic qualities for use in integrated circuits; therefore, as a technology that has actually headed the list of post Si technologies in this field since the 1980s, their development has been pursued vigorously, inclusive of HEMTs and p-HEMTs in particular because of their mobility characteristics. However, in the end, they have not been able to replace MOSFETs and have stopped at applications in discrete and small scale integrated circuits for high frequency, high-speed fields as described above. Therefore, the problems of substrate cost caused by using scarce elements compared with that chemically, mechanically and economically superior crystal material Si, by the difficulty of controlling the peculiar stoichiometry of the chemical compounds, mechanical embrittlement and poor thermal conductivity characteristics as well as several industrial factors such as the difficulty of improving quality have been influential. However, from the technical standpoint of devices, the absence of the stable MOSFET technology in group Ⅲ-V compound semiconductors can be thought of as one of the major factors. GaAs FETs or HEMTs surpass Si MOSFETs in simple device speeds if they have the same designs because of their high mobility. However, these differ from simple devices typified by the high frequency switches described above or small scale integrated circuits, and in large scale integrated circuits, there have been problems not only with speed in simple FETs, but also with delays that accompany charging and discharging of parasitic capacitance in the charging and discharging capacitance of the FET group that is connected to the next FET group and the wiring that makes these connections. In particular, the point about interconnection capacitance is a serious problem, and it can be assumed that, in the end, radical measures such as optical wiring, which will be discussed in the following, will be necessary. First of all, sufficient output current from the transistor must be supplied from the transistor to wiring in which the resistance has been reduced as much as possible. Therefore, the current density of simple transistors must be increased, and when the mobility has reached a fixed limit, the necessary current drive capacity must be assured by increasing the gate capacitance and raising the channel electron density thereafter. This has been accomplished by making the Si gate oxide layers, which have a high level insulating performance, thinner and miniaturized in Si MOSFETs. However, as was shown at the beginning of this section, in GaAs FETs or HEMTs that use Schottky gates, there is a limit to gate voltage amplitude

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because high gate voltage resistance cannot be achieved. The maximum channel electron density is held to a value less than that for Si MOSFETs by a factor of 10. The further miniaturization progresses, the smaller the possible voltage amplitude becomes, and the advantage of high mobility is lost.

3. GaAs interface state origins and achievement of nMOSFETs

On the one hand there are the developments and limitations of HEMT technology that have been described above, but investigations into MOS interface control in GaAs have continued, and as a result, normally-OFF surface inversion nMOSFETs have already been achieved, even though it is only on the research level. It can be assumed that the following two technologies have contributed to this development. First, the group of Hong et al. at Bell Laboratories made clear the possibilities for elimination of pinning at Ⅲ-V MOS interfaces by molecular beam epitaxy (MBE) growth of a Ga_2O_3/Gd_2O_3 single crystal layer on GaAs in a series of studies starting in 1996.[11), 12)] The proof of this "existence theorem" became the motivation for a series of studies that followed. Second, what should be raised is the development of high dielectric constant (high-k) insulating film technology. A variety of MOS devices (logic, memory, sensors and power) that use Si have been made practical, but one of the reasons for this success is that a SiO_2/Si structure provided with high insulating properties and excellent interface characteristics can be fabricated by the simple method of thermal oxidation of Si. In terms of these interface characteristics, the fact that the uncombined hands (dangling bonds) of Si atoms in the SiO_2/Si interface are a primary factor in the interface state is clear from electron spin resonance measurements.[9)] The density of these dangling bonds is comparatively high at approximately 10^{12} $cm^{-1}eV^{-1}$ directly after thermal oxidation, but technology has been established to be able to reduce it to the 10^{10} $cm^{-1}eV^{-1}$ level or less by carrying out heat treatment in a hydrogen atmosphere. However, along with the scaling limitations discussed at the beginning and in a situation where it is difficult to handle miniaturization of MOSFETs simply with oxidation films as well as from the necessity for controlling gate leaks accompanying miniaturization of logic LSIs and dealing with increases in the capacitance of the dram capacitors, there have been rapid advances in techniques for growth using deposition methods such as chemical vapor deposition (CVD) and atomic layer deposition (ALD) for high quality, high-k metal oxide layers in place of thermal oxidation layers. Along with progress in measurement and simulation technology for evaluating and understanding the structure and physical properties of MOS interfaces, it is possible to form insulating layers while controlling the underlying substrate and interface structure (oxidation state in particular).

There have been many studies of mechanisms arising in the metal-semiconductor (MS) interface between the semiconductor and metal, and as a result, excellent reviews have been brought together.[13)–15)] The main models for explaining the origin of the interface state is the metal induced gap state (MIGS) model, unified defect (UDM) model, disorder induced gap state (DIGS) model, effective work function model, bond polarization model and others. Just which model is suitable for which system is still being debated at this point, but at the very least, the occurrence of interface states due to the MIGS mechanism has been verified by calculations for the MS interface, and this model is widely accepted.

Among the five models above, Spicer's unified defect model[16)] and Hasegawa's DIGS[17)] model (**Fig. 9**) are applicable to MOS interfaces. The concept of the former is that the causes for the type control to are found in local structures, and besides structures such as dangling bonds in the SiO_2/Si interface, vacancies where group Ⅲ atoms and group V atoms are missing, antisite defects where group V atoms are in group Ⅲ atom sites (or vice versa) and dimer structures where group V atoms are bonded to each other are also thought of as origins of the interface state. The concept of the latter

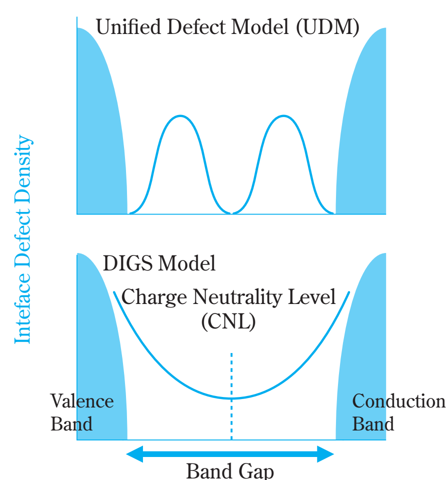

Fig. 9 Unified defect model and DIGS model

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is that, as a result of the junction of solids themselves being the origin of the crystal bond state, the electronic states of the valence band and conduction band exude into the gap and form the state in the gap. In other words, structural changes on a larger scale than conceived of in the unified defect model are thought of as the origin of the interface units. The defects conceived of in the unified defect model each have their own intrinsic energy; therefore, peaks appear in the interface state spectrum. On the other hand, from the components of the interface state in the DIGS model, the density gets smaller moving away from the band edge toward the middle of the gap; therefore the pattern is U-shaped. If the state is occupied up to the energy at which the interface state is the smallest, the charge of the interface can be thought to be neutral; therefore this energy is called the charge neutrality level (CNL).

Let us take a look at the correspondence between the main experimental facts concerning the III-V interface state formation and the pinning model described above. First, as Spicer, who proposed the unified defect model, reported early on, a clean GaAs (110) surface is prepared by cleavage in a ultrahigh vacuum, and if this is allowed to absorb oxygen atoms, Fermi level pinning will already be formed at a low coating rate of a 0.05 atom layer (**Fig. 10**).[16] In addition, when MOS capacitors are fabricated by forming an insulating film on the surface of a group III-V compound semiconductor by deposition, the insulating film is grown after removing the natural oxidation film from the surface.[18] An atomic layer deposition (ALD) insulating film is formed[19] using starting materials that have a reducing effect on the surface oxide film to obtain excellent characteristics. This suggests that the inducement of the defects is dependent on a local structure binding oxygen and the group III-V compound semiconductor, and these experimental results support the unified defect model.

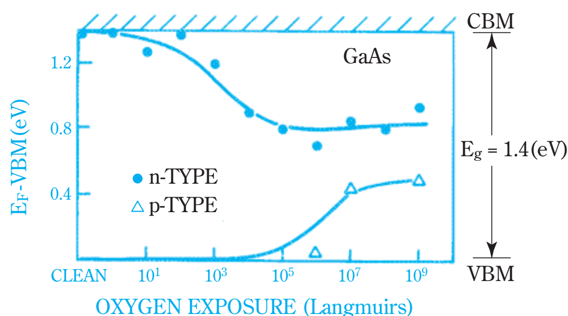

Fig. 10 Fermi level pinning by oxygen exposure on GaAs surfaces[16]

On the other hand, as was described earlier, even if the Ga_2O_3/Gd_2O_3 oxides are formed on top of GaAs (in other words, the bonds are formed between the oxide and GaAs), the fact[20] that pinning is not brought about if this is epitaxial supports the DIGS model that says that this order in the crystals of the group III-V compound semiconductor is the cause of the interface state (**Fig. 11**). According to research over the last several years, MOS operation is comparatively easy with group III-V compound semiconductors containing In. In other words, it has been shown that the interface state density in the neighborhood of the conduction band is comparatively low. With group III-V compound semiconductors containing In, it is known that CNL is generally in the neighborhood of the conduction band (**Fig. 12**), and the experimental facts can also be explained by the DIGS model.

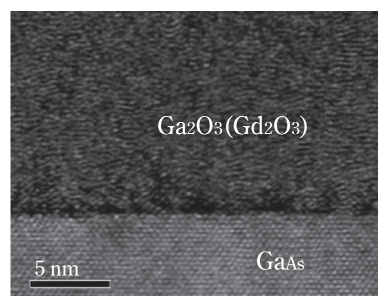

Fig. 11 Epitaxially grown Ga_2O_3/Gd_2O_3 on GaAs[20]

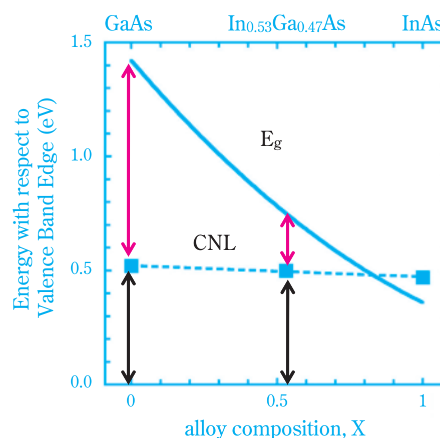

Fig. 12 Energy level for charge neutrality level (CNL) in $In_xGa_{1-x}As$

Furthermore, the interface state is present not only in the band gap, but also within the bands, and it has been pointed out that this affects the device characteristics. Investigations are starting into the details of this. A trap state in a band is difficult to explain with the

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DIGS model, and this should be thought of as deriving from defects. In terms of the various defect structures that can be conceived of with the unified defect model, the energy states have been quantitatively estimated by calculations,[21] but qualitatively they are understood as shown in **Fig. 13**. Group III-V compound semiconductor crystals are formed by bonding in which the sp^3 hybrid orbitals of the group III atoms and group V atoms participate. At this time, the energy of the sp^3 hybrid orbitals of the group III atoms is higher than that of the group V atoms; therefore, the bonds between the atoms have characteristics of both covalent bonds and ionic bonds. Since group IV semiconductors are formed only by covalent bonds, the bonding state for the covalent bonds aggregates in the valence band and the antibonding state in the conduction band. However, because of the ionic nature of group III-V compound semiconductors, they are strongly characterized by the valence band being an aggregation of the p orbitals of the group V atoms and the conduction band being an aggregation of the s orbitals of the group III atoms. Here, an oxide film is formed on the group III-V compound semiconductor, and bonding arises between the group III atoms and oxygen and between the group V atoms and oxygen. The oxygen bonds of the group III atoms are strongly ionic, and a wide gap is formed between the bonding state and the antibonding state. These states are respectively within the valence band and conduction band of the group III-V compound semiconductor. On the other hand, the bonds between group V electrons and oxygen have stronger covalency, and other than cases where the group III-V compound semiconductor is a nitride, the bonds between the atoms have different periods (different sizes of orbits); therefore the difference in the energy for the bonding state and antibonding state is not very large. Therefore,

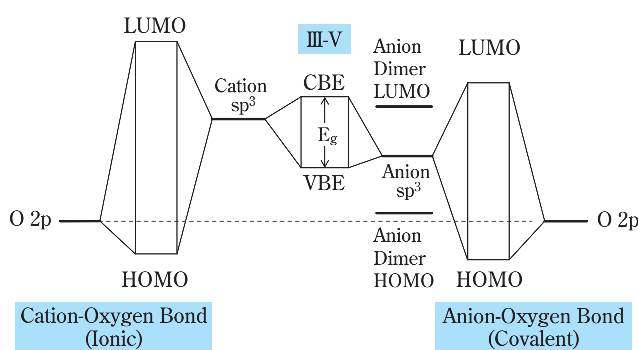

Fig. 13 Energy diagram for III-V semiconductors, cation/anion oxides and anion dimer.

the antibonding state of these bonds is expected to form a state comparatively near the conduction band edge for the semiconductor. In addition, as can easily be imagined from this diagram, the dangling bonds of group III atoms give rise to the state near the valence band of the band gap, and on the other hand, the dangling bonds of the group V atoms give rise to the state near the conductive band edge of the band gap. In addition, if dimers where group V atoms are bonded to each other are produced, their antibonding state can be assumed to be positioned close to the conduction band.

4. Recent developments in III-V MOSFET technology

MOSFET operation has been achieved in compound semiconductors, starting with GaAs, which has been an issue for many years, but while, on the other hand, we are reaching the limits of miniaturization in Si CMOS integrated circuits, it can be said that a fusion of the two is a technological necessity. Therefore, starting in the second half of the first decade of this century many research and development programs were started almost at the same time in Japan, the United States and Europe, and a vigorous development competition began.

As a technology booster capable of improving CMOS performance after running into the limitations of miniaturization, research and development on group III-V compound semiconductor channel transistor technology on a silicon platform has been moving forward through consignments at Tokyo University, the National Institute of Advanced Industrial Science and Technology (AIST), the National Institute for Materials Science, Sumitomo Chemical Co., Ltd. under the New Energy and Industrial Technology Development Organization (NEDO) project "Development of Novel Materials for Nanoelectronics Semiconductor Materials and Novel Structured Nanoelectronic Device Technology" (FY 2007–2011). The main results up to now will be introduced in the following.

The following problems exist for achieving group III-V compound semiconductor channel transistors on the large silicon platforms that are currently the actual basis of industrial integrated circuit production lines.

- MOS interface control technology
- Source and drain forming technology
- Integration on Si substrates
- Achieving CMOS technology through the realization of high performance nMOS and pMOS.

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(1) MOS interface forming technology

One of the most essential problems up to now has been obtaining MOSFETs on a level where there is no interference in ON/OFF operations due to several elemental technologies by developing various technologies in recent years as described above. It is known that low interface state density MOS interfaces can be formed by forming Ga_2O_3/Gd_2O_3 on clean surfaces by suitable methods even with GaAs, but it is possible to form high quality MOS interfaces easily by using InGaAs. After InGaAs crystal surfaces formed by epitaxial growth on InP substrates are cleaned by chemical treatment, S or Se treatment or a nitriding treatment is carried out. Thereafter, an Al_2O_3 gate insulating layer having excellent interface characteristics can be formed by deposition of an Al_2O_3 film using atomic layer deposition (ALD). The exact mechanisms for these processes have not been verified yet, but they are presumed to be elimination of excess As or As oxides, which are presumed to be factors in the interface state, through these treatments (it can be assumed that reduction and elimination of surface oxide films by the starting material trimethylaluminum (TMA) in the S/Se and nitriding treatments and initial ALD process makes a contribution) and, further, simultaneous progress at the terminals (S/Se, nitriding) of the surface dangling bonds. In addition, with InGaAs, as is shown in **Fig. 12**, the CNL is close to the conduction band, and the lower edge of the conduction band is further away from the vacuum level than that of GaAs (larger electronegativity); therefore, the interfacial levels originated in the antibonding state of interface bonds which is shown in **Fig. 13** go into the conduction band, not forming those state in the forbidden gap, and result in relatively better MOS interfacial characteristic in InGaAs. Because of this series of operations, there was success with the operation of n type InGaAs MOSFETs having electron mobility two to three times higher than the Si MOSFETS that are generally used (**Fig. 14** (a)).[23]

It is a fact that the InGaAs MOSFET electron mobility observed above is still lower than that of HEMTs having the same channel materials. Since this varies sensitively according to the surface treatment method (S treatment, Se treatment, etc.), it is presumed that in addition to being affected by the residual interface state, which is the electron scattering center even now, the greater local fluctuations in the dipole that forms the cations (In, Ga) and anions (As) present in the interface, are also influential, in contrast to Si, which is formed from a single constituent element. The data above is results with (100) crystal surfaces, which are typically used, but the substrate surface orientation for the original crystal is changed to an (111) A surface, and the channel electron mobility is greatly improved by carrying out suitable pretreatment (**Fig. 14** (b)).[24] In this case, the atomic planes of the cations (In, Ga) in the neighborhood of the MOS interface are aligned, and in this case, the fact that the dipole described above is hardly formed in a direction within the plane, or the fact that the anions (As) themselves, which have an important role in forming the interface state, have little effect probably contribute.

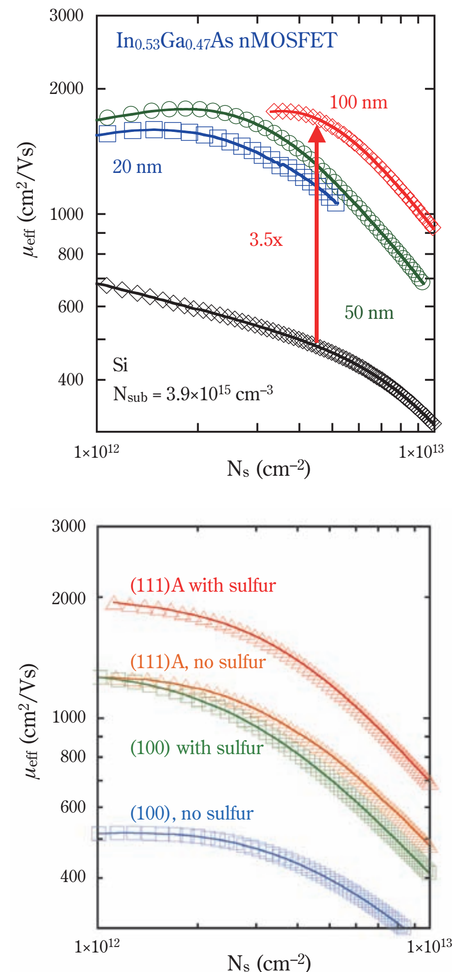

Fig. 14 Mobility (μ_{eff}) carrier concentration (N_s) characteristics for InGaAs MOSFETs.
(a) InGaAs-OI structures with InGaAs (100) channel thickness of 20, 50 and 100 nm
(b) μ_{eff} for InGaAs MOSFETs on different InGaAs surfaces.[24]

In addition, for another approach, a structure in which an InP crystal layer, which has a smaller electron affinity than the channel InGaAs is thinly embedded

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between the gate insulating layer surface and channel surface in the same manner as HEMTs. A two-dimensional electron layer is induced on the channel layer side by applying a positive electric field to the gate electrode, but the electrons that are first introduced in the InGaAs layer, which has a large electron affinity like HEMTs, are physically separated from the MOS interface, which includes a residual defect state, by the InP layer; therefore, the mobility is greatly improved again, and peak mobility exceeds 5000 cm^2/Vs.[25] However, if the InP layer is excessively thin, improvements in the gate capacitance, which is the original intention of MOS (improvement in electron density), becomes difficult. However, with group Ⅲ-V compound semiconductors, which can be applied in a greater variety of heterojunction technology than Si, the possibilities for various improvements using high-level heterojunction control in MOSFETs can be considered in the future.

(2) Low resistance source and drain forming technology

As was described in the earlier section on high-frequency switches, the importance in actual devices of also having reduced channel resistance is reducing the access resistance from the source and drain electrodes to the channel. In general, the formation of source and drain ohmic electrodes in group Ⅲ-V compound semiconductors is typically done by the formation of alloyed electrodes on a contact layer doped at a high concentration, which is epitaxially grown in advance, and combinated with recessed structures in the normal p-HEMT process, but such a process can hardly be applied to MOSFETs, which is basically a planar process. Thus, a method where, before the formation of this gate layer, the impurity is implanted at a high density by ion implantation, activated by heat treatment and the ohmic electrode formed is most commonly used. However, at present, there is the problem of a parasitic resistance that is a factor of 10 higher than the necessary value because of damage to the crystal by the implantation process or not reaching an effective impurity concentration. On the other hand, in Si MOSFETs, source and drain forming technology that makes use of the formation of metallic compounds (silicides) with Si by Ni and many other metals is typical. Though it was not known conventionally, we found for the first time, as a result of research in a project consigned to us, that metallic compounds were produced by forming alloys in the same manner as Si and Ge as a result of carrying out low temperature heat treatment,[26] and, using this, it was possible to form a InGaAs MOSFET having low-resistance, self-aligning metal source and drain electrodes for gates.

(3) Technology for forming Ⅲ-V MOSFETs on silicon wafers

Heteroepitaxial growth of group Ⅲ-V compound semiconductors on single crystal silicon substrates has been a problem for many years. The formation of highly functional group Ⅲ-V compound semiconductors on Si, which is inexpensive and mechanically superior in large sizes, is very appealing from the standpoints of costs and functions; therefore, research and development has been going on actively since the 1970s, just like GaAs MOSFETs. However, this also has a history of falling into calamity like MOS. When growing polar GaAs, which is formed from two elements on a Si crystal, which is a nonpolar crystal formed from a single element, an antiphase domain in which Ga layers and As layers come in alternately arises, and crystallinity is lost remarkably since there is a large difference between the coefficients of thermal expansion for the two, a large thermal strain arises in heat treatment processes including crystal growth processes, and at room temperature, sometimes destroying the crystals. There are problems with their contaminating each other because they have a dopant relationship (impurity) with each other, and these have prevented them from becoming practical. In recent years, we have seen the far-off glow of a solution from two different approaches. One of them is a system of forming a mask on the Si substrate and carrying out epitaxial growth selectively in an extremely limited area, and the other is a system of separating only the high quality epitaxial crystal layer from a substrate after epitaxial growth on a separate substrate in advance and bonding it to the Si.

In general, a large number of initial nuclei are generated by heteroepitaxial growth on a different type of substrate, and growth is aggregated within subtly different phases for each of these nuclei. However, this is a cause of the antiphase domain problem and misfit dislocation. The basic principle of the former (selective epitaxy) system is single domain growth from one developmental nucleus by limiting the growth area to a very minute area. Even when dislocations arise, the fact that the dislocations are moved outside of the crystal and disappear is widely known in the field of metallurgy, and it is a method for exploiting GaAs on Si.

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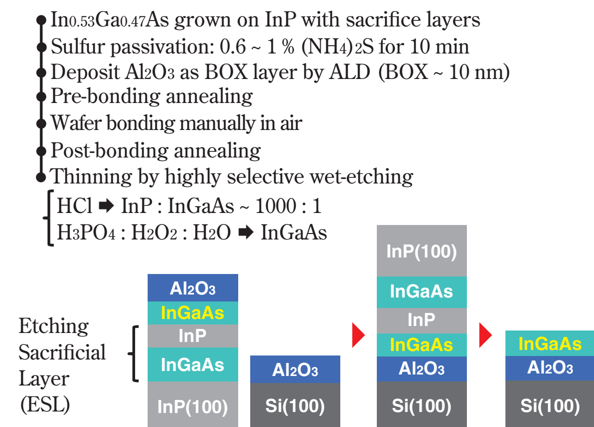
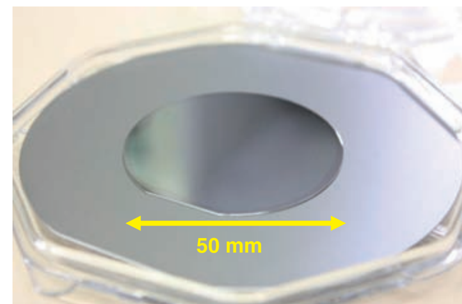
However, since the distance to the side surface for dislocations escaping is extremely small with microcrystals, it is possible to effectively increase the effect of heat treatment. In addition, in terms of the difference in coefficient of thermal expansion, one of the merits is that it is difficult for the fracture stress to work for crystals that are finely divided in advance. The difficulties with selected epitaxy are the shape and configuration of the growth area being sharply affected by composition, crystal shape and concentration of impurities in the generation of initial nuclei and epitaxial growth thereafter, and controlling these is not easy.

On the other hand, the latter (bonding system) has few problems in terms of crystal quality, but separation from the original substrate, and in particular, separation of thin crystal layers, is the most important problem in handling this.

In our consigned research, we also worked on both systems from the beginning of our investigations, but the details will be omitted here. As an example, the results for InGaAs MOSFETs on Si substrates using the bonding method and a combination of the MOS interface control and drain and source forming technology described above will be introduced.[23), 26)]

Fig. 15 shows the process flow used this time. An Al_2O_3 ultrathin film formed by an ALD was used for forming the gate oxide film, but this oxide film has superior adhesion strength in its junction with the Si substrate. After the formation of an Al_2O_3 thin film by ALD on the surface of a thin InGaAs epitaxial crystal layer formed by MOCVD on an InP single crystal substrate in this process and after bonding to the Si substrate at normal temperatures, only the InGaAs epitaxial layer remained, and the InP substrate was removed by selective etching. Thereafter, an InGaAs channel MOSFET having an Al_2O_3 thin film MOS film was formed using the MOSFET forming process we developed on the InGaAs crystal layer on the Si. The source and drain had a metal source-drain structure using the metalization reaction with metallic Ni described previously. **Fig. 16** shows a TEM image in the neighborhood of the completed MOSFET channel. There are several variations for the thickness of the channel InGaAs crystal layer, but the thickness is accurately controlled by matured MOCVD film forming technology, and an ultrathin channel with a minimum thinness of 3.5 nm was formed over the entire surface of the wafer and MOSFET operation was successfully demonstrated. In this process, the surface bonded to the Si substrate uses the same process as MOS gate forming, and an Al_2O_3 adhesion layer is formed; therefore, the interface on the substrate side (adhering side) also has excellent electronic characteristics. The MOSFET OFF-state characteristics can be improved further by the use of an unaltered low resistance Si substrate for back gate electrodes. InGaAs MOSFETs on insulating films having these ultrathin channels are an important elemental technology for future ultrahigh speed MOSFETs.





• 2-inch $In_{0.53}Ga_{0.47}As/Al_2O_3$-Si wafer
• Smooth and mirror surface.

Fig. 15 Process flow for wafer direct bonding in fabrication of InGaAs on insulator (OI), and appearance of bonded wafer.

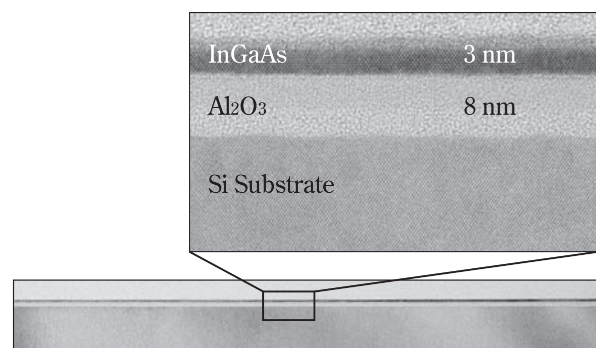


Fig. 16 Cross-sectional TEM view of ultra thin InGaAs channel on insulator.

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Above, we have described n type MOSFETs that make use of InGaAs and have high electron mobility. On the other hand, at present, for p type MOSEFETs, which are another element for complementary circuits, the use of Ge, which has the highest hole mobility among the various semiconductors, is thought of as being a powerful solution. The elemental technology for this has already been accomplished in projects like Millennium Research for Advanced Information Technology (MIRAI), but in our current consigned research, we are also investigating integration of Ge MOSFETs, but we will omit the details here.

NMOS and PMOS that achieve mobility that exceeds silicon have already been realized with surface inversion MOSFET operation by resolving Fermi level pinning as touched upon above. Moving forward, the problems are actually achieving high current driving force when miniaturization has gone to the same size as the most advanced Si ULSIs, controlling OFF current and variations and achieving decreased power consumption.

5. Future problems for positioning new material channels in ITRS

The International Technology Roadmap for Semiconductors (ITRS) has been published (http://www.itrs.net/) based on surveys and discussions among the experts in the field of semiconductors in the United States, Europe and Asia. In the ITRS, the performance that should be achieved by LSIs and other semiconductor products is shown for each year in the form of specific target values, and also the technical problems necessary for realization of these and the resolutions that can be considered at that point in time are summarized. According to ITRS 2010, the latest version for 2010, at the current time, the miniaturization of LSIs in the future will develop with control of the short-channel effects by SOI structures and finFET structures on the one hand, and on the other, the introduction of group III-V compound semiconductors and Ge high mobility channel materials is envisioned around 2018 when gate lengths are expected to go under 10 nm (**Fig. 5**).[4] Up to now, high mobility channel materials have mainly been handled in the Emerging Research Devices section that targets long-term technical problems. Along with Si CMOS miniaturization becoming technically more difficult, expectations for equivalent scaling are increasing as we move forward. It is predicted that, the target values that must be satisfied by high mobility channel MOSFETs for replacing silicon, particularly silicon with the mobility increased by applying strain, will be clarified. The problems for the future that are common to both group III-V compound semiconductors and Ge are arranged in the following. First, it is necessary to further increase the quality of MOS interfaces and further reduce the resistance for the source and drain as elemental technology for achieving device performance that sufficiently utilizes high mobility. For the former, interface state occurrences must be controlled over a wide range of energies, and efforts must continue for minimizing carrier scattering. For the latter, it has been reported that resistance can be reduced by forming the source and drain using regrowth. However, it is thought that metal sources and drains will be effective from the standpoint of production costs, and it is thought that research should move forward aimed at improving the characteristics of these.

In addition, the key to introducing high mobility channels into silicon platform technology, which has achieved high levels, is establishing mass production technology for forming group III-V compound semiconductor / Ge channel layers on silicon and controlling mutual contamination by elements (particularly contamination by group V elements originating in the channel formed by a group III-V compound semiconductor). Furthermore, the integration of conventional silicon processes that include high temperature processes at roughly 1000°C and III-V / Ge processes that typically must be carried out at temperatures of around 400°C or less can also be thought of as an important problem.

Future Prospects for New Technology

Within the past 40 years of transistor scaling, there have been dramatic improvements in simple transistors. On the other hand, as scaling has progressed, the performance of LSIs as a whole has improved, and problems with wiring delays have escalated. This is because wiring resistance (R) and load capacitance (C) arise because of the reduction in the cross-sectional area of wiring, and the so-called RC delays are in turn increased. The effects of increased delay time in global wiring, where the wiring is the longest, have been exposed in recent years in the form of LSI operating clock speed saturation. Increases in wiring delays can be controlled to a certain extent by introducing repeaters, but there are problems with superfluous chip area and power consumption. Therefore, investi-

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gations into the introduction of optical wiring have begun in recent years. **Fig. 17** shows the results of comparing the relationships between the power delay product and wiring length for optical wiring and electrical wiring.[27] As is shown in this figure, there are expectations for the performance of wires to exceed the performance of current Cu wiring in wire lengths greater than several mm with the development of technology nodes. Thus, by introducing optical wiring, signal delay can be reduced without the effects of wiring resistance and capacitance. In addition, since the frequency of light is roughly 200 THz, the signal band per wire can be greatly improved by using wavelength multiplexing technology. Furthermore, since no crosstalk due to electromagnetic induction is present, design layouts with increased wiring density and flexibility are possible, so there are expectations for achieving ultra high-speed global wiring networks not dependent on wiring length. In addition to this situation, there have been rapid developments in research on Si-based optical devices, so-called Si photonics, and research results on optical waveguides, lasers, optical modulators, photodetectors, etc. that make use of fine line silicon have been reported by universities and industry in the United States and various countries in Europe. The momentum for achieving optical wiring Si LSIs with Si CMOS and optical devices integrated monolithically has explosively increased. On the other hand, in contrast to silicon development, research is moving forward actively to fuse Ge and group Ⅲ-V compound semiconductors, which have a band gap suitable for this wavelength band, with an Si platform to achieve semiconductor lasers and transparent photodetectors for the 1.3–1.55 μm wavelength band that is used in optical fiber communications. With advances in CVD technology, technology for forming Ge, which is also a group IV semiconductor, on a Si platform has progressed, and many Ge photodetectors, etc., using high quality Ge layers in which crystal defects due to lattice mismatching have been controlled have been reported. LUXTERA and other American ventures have started to make them practical. Since Ge is a high mobility material that has electron mobility twice that of Si and hole mobility four times that of Si, there are expectations for it as a channel material for high performance MOS transistors, and achievement of high-performance photo-electron LSIs with monolithic integration of high-performance Ge CMOS and Ge photodetectors is expected. We were successful in prototyping a device with a monolithic integration of a Ge MOSFET and SiGe photodetector on a Si platform using an oxidation concentrating process capable of achieving a germanium on insulator (GOI) structure by oxidizing SiGe grown on a SOI substrate (**Fig. 18**).

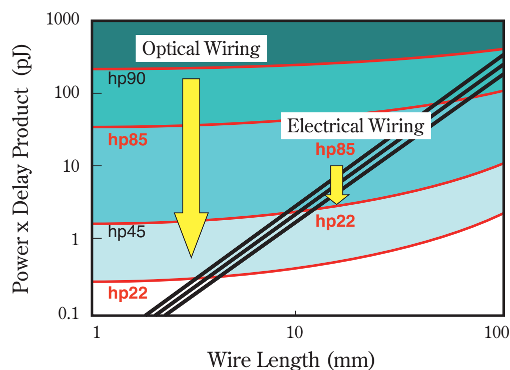

Fig. 17 Comparison of power/delay in electrical wiring and optical wiring[27]

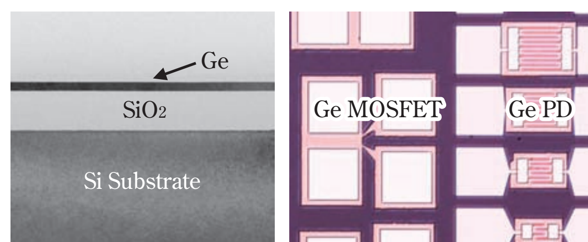

Fig. 18 Ge/electro-optical integrated circuit

On the other hand, research is progressing on integration of InP/InGaAs semiconductors, which have superior light emitting functions and optical characteristics for achieving light emitting elements such as semiconductor lasers and higher performance optical modulators and photodetectors, on a Si platform. Attempting crystal growth of group Ⅲ-V compound semiconductors directly on Si substrates has been studied for a long time, but further crystal quality improvements are required for making them practical because of the large lattice mismatching, etc. On the other hand, a research group of the University of California at Santa Barbara (USCB) and Intel Corp. reported the world's first hybrid laser that combines a group Ⅲ-V compound semiconductor light emitting layer and Si fine line optical wave guide by bonding InP/InGaAs semiconductor on to a SOI substrate in 2005 (**Fig. 19**).[28] In addition, a Ⅲ-V on insulator (Ⅲ-V-OI) substrate that can be used in group Ⅲ-V compound semi-

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conductor photonics by wafer bonding of a thermally oxidized Si substrate and InGaAsP/InP substrate has been reported, and ultrasmall InP optical devices have been achieved (**Fig. 20**).[29] Currently, research on technology for integration of group Ⅲ-V compound semiconductors on Si platforms using wafer bonding is developing dramatically, and not only semiconductor lasers, but also various Ⅲ-V/Si hybrid optical devices, such as optical modulators and photodetectors, have been reported. Since group Ⅲ-V compound semiconductors have extremely high electron mobility, there are expectations for them as the next generation of MOS transistor channel materials along with Ge, as touched upon in this article. Research on logic MOS transistors, quantum tunnel transistors, which can operate on even tinier voltages, etc., using group Ⅲ-V

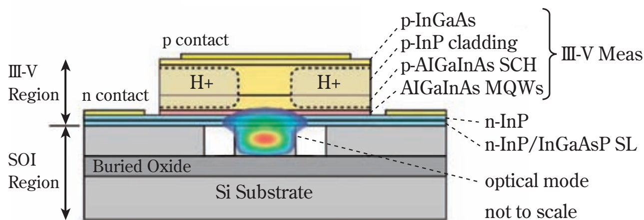

Fig. 19 Ⅲ-V/Si hybrid device integrated on SOI [28]

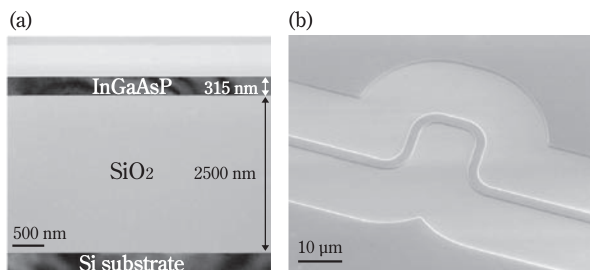

Fig. 20 (a) Cross-sectional TEM images of Ⅲ-V-OI substrate [29]
(b) Sem image of bent waveguide with 5 µm bend radius [29]

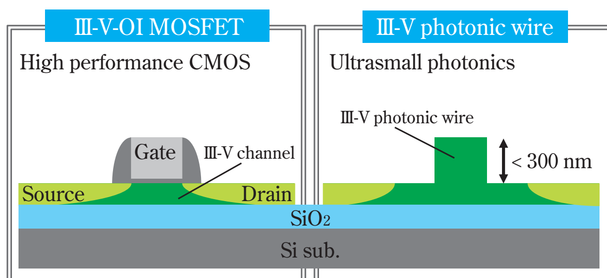

Fig. 21 Ⅲ-V CMOS photonics platform integrated on SOI

compound semiconductors is accelerating worldwide. Ultrasmall group Ⅲ-V compound semiconductor optical devices on Ⅲ-V on insulators formed on Si substrates and Ⅲ-V CMOS photonics platforms (**Fig. 21**) with monolithic integration of high-performance Ⅲ-V CMOSFETs can be thought of as the ultimate form of future ultrahigh speed ULSIs.

As was noted at the beginning of this article, integrated circuits have achieved both increased speed and increased integration with semiconductor device miniaturization following the scaling rules as a major driving force. Gordon Moore, one of the founders of Intel Corp., which is a leader in ULSIs characterized by high speed and high level of integration and microprocessors, stated that integrated circuits would double in the rate of integration roughly every 24 months, and the so-called Moore's law has also been an empirical rule up to now. It has also been a powerful guideline for the development of integrated circuits. If this law continues, the level of integration in the most advanced ULSIs will exceed 15 billion devices (roughly equal to the number of neurons in the human brain) within the next 10 years, but on the other hand the orientation of development has begun to branch in several directions. One is the route of "more Moore," in other words, exhausting the essence of miniaturization technology taking strength from the several technology boosters have been described in this article, and further, moving forward with three-dimensional integration and increased speed, moving from conventional two-dimensional planar devices toward three dimensions, continuing with Moore's law. Another one is now called "more than Moore," and the definition is, instead of Moore's law, which will come to an end eventually, we should go beyond the logic circuit framework centered on conventional CMOS technology and pursue new technologies based on different operating principles or design concepts. This is the route of searching for new embryonic breakthroughs such as spintronics, which makes use of the spin of electrons, optical computers, quantum computers, and even further, biological brain models. On the other hand, as a route for a comparatively narrow definition of "more than Moore," there is technology for combining semiconductor technologies having functions different from the digital logic circuits up to now while using of similar semiconductor technology, and this development has already progressed to the product level. Technologies that can be combined include memory, optics, high frequencies, electric

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power, microelectromechanical systems MEMS and biotech functions. System LSIs that combine memory functions with digital logic circuits have already been made practical since early on. In addition, as was explained in the last section of this article, overcoming wiring delay centered on communications devices is being pushed forward for optical functions also, and the range of applications has gradually extended from the original long-distance communications to communications between systems, between boards and between dies. Presently, the wiring within dies has become a real possibility, and we are at the stage where work is being done. This route encompasses work on functions with direct processing of optical signals, and in the end, technology that could develop into optical computers, which is out of the wider definition of "more than Moore," can be considered. In addition, the final fusion with high-frequency wireless communication functions which are the connection means for user terminals can be thought of as an important area for technological development for moving forward with the integration of different functions into integrated circuits along with electric semiconductor technology and MEMS technology that has been pushing forward different forms of progress in fields with both the same and different functions. Furthermore, fusion with biotechnology which has pushed forward remarkable development since the previous century along with semiconductor and computer technology is expected to become necessary in the future for forming interfaces with living organisms, which are the final "connection" partners for semiconductors. We must have a deeper understanding and control over these various different materials to achieve integrated circuits in a higher dimension through the fusion of different materials such as the extremely advantageous platform material and technology of Si and other various types of semiconductor materials and biomaterials.

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PROFILE

Masahiko Hata

Sumitomo Chemical Co., Ltd.
Advanced Materials Research Laboratory
Senior Research Specialist

Dr. Mitsuru Takenaka

The University of Tokyo
Department of Electrical Engineering
Graduate School of Engineering
Associate Professor

Dr. Shinichi Takagi

The University of Tokyo
Department of Electrical Engineering
Graduate School of Engineering
Professor

Dr. Tetsuji Yasuda

National Institute of Advanced Industrial Science and Technology
Integration Group Leader
Deputy Director of Nanoelectronics Research Division & New Materials and Functions

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