Development of GaN Single-Crystal Substrates

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In this paper, we first review various fabrication technologies for GaN single-crystal wafers which have been reported to date. Then, our original fabrication technique for GaN single-crystal wafers called void-assisted separation (VAS)-method is introduced. Our recent progresses in GaN wafer fabrication technology for next-generation devices, such as further improvement of GaN crystal quality as well as increasing wafer size, are also explained in detail.

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Introduction

Compound semiconductors have excellent light emission characteristics and controllability of wavelength of emitted light by adjusting alloy composition, which are not available with Si. Therefore, various kinds of optical devices such as light emitting diodes (LEDs) and semiconductor lasers (LDs) have been realized using compound semiconductors, and applied to display back-lighting and illumination, light sources for projectors, and optical pickups for reading and recording of CDs and DVDs. Furthermore, because of their excellent electrical characteristics, they are also used in electronic devices for high-frequency amplifiers in mobile phones and smart phones, as well as for amplification devices in ground stations for mobile phones, making them an indispensable core material supporting the current IT society.

Regarding III-V compound semiconductors, GaAs and InP substrates were developed at first together with materials that could be grown on them, i.e. materials containing Ga, In, or Al for group III, and As, P, or Sb for group V. They have been used to realize LEDs and LDs covering infrared to yellow-green spectral range, as well as high-frequency electronic devices. SCIOCS Co., Ltd. has also been developing bulk crystal growth technology of the main III-V compound semiconductor, GaAs, and epitaxial growth technology for fabricating optical and electronic devices on them since the era of its predecessor Hitachi Cable Co., Ltd. The GaAs substrates and GaAs-based epitaxial wafers developed by us have made a large contribution to the development of the present IT society.

On the other hand, in the 1980s, Akazaki, Amano, Nakamura, et al., who won the Nobel Prize in Physics in 2014, succeeded in developing gallium nitride (GaN) and opened the pathway to achieving LEDs and LDs that emitted light in the ultraviolet through green range.[1)–4)] As described above, devices formed from conventional GaAs and InP have been formed by epitaxial growth of device structures on the same types of substrates formed from GaAs and InP. This is because these materials can form melts at high temperatures, and bulk crystals can be obtained by their solidification process; therefore, single crystal GaAs or InP substrates can be achieved. On the other hand, since GaN systems have a high equilibrium partial pressure for nitrogen, growth of GaN ingots from a melt is practically impossible. Therefore, GaN devices were realized at first through technology for growth of thin-films on foreign substrates such as sapphire or SiC.[1), 2)] In these cases, the resultant GaN film inevitably contained high

threading dislocation density (TDD) of 10^8–10^9/cm^2 due to differences in the lattice constant and thermal expansion coefficient between the GaN layer and the substrate. In the case of conventional semiconductors, such a high dislocation density would have fatal effects on device operation. However, fortunately, the dislocation effects are not serious in GaN-based LEDs because the unique active layer material of InGaN which gives strong carrier localization can be used. As a result, GaN-based white, blue and green LEDs have been realized.[3] However, for LDs, which are operated under much higher current level than LEDs, device life depends strongly on TDD and, hence, single-crystal, free-standing GaN substrates having lower TDDs were required. Therefore, in the latter half of the 1990s, development began on methods for fabricating GaN single crystal substrates using a variety of methods.[5), 6)]

Also at SCIOCS Co., Ltd. in 2001, we developed an original fabrication method for GaN single crystals named void assisted separation (VAS), where a thick, main GaN layer was grown on a thin GaN-seed layer containing high-density, nanometer-sized voids formed on a sapphire substrate, and the main GaN layer was separated from the sapphire substrate at the void parts after growth, resulting in a formation of a free-standing GaN substrate. This method can realize GaN single crystal substrates having uniformly distributed dislocations with low TDD (in the lower half of the 10^6/cm^2 level), as explained in detail in the following section.[7)–12)] Because such a GaN substrate having uniform dislocation distribution had never been realized by other fabrication method available at that time, it has been widely used for various applications including blue LDs.

Furthermore, GaN-based materials has been also considered promising for power devices from the beginning of their development because of their high breakdown electric field and mobility. Since operation under large current levels is also required in this case and, hence, a narrow bandgap InGaN layer cannot be used, there is great merit in using high quality GaN single crystal substrates. Therefore, commercialization and stable supply of high-quality GaN single crystal substrates by several companies including SCIOCS Co., Ltd. are now accelerating the development of GaN-based power devices.[13), 14)] As examples of devices realized on free-standing GaN single crystal substrates, schematic representations of a blue LD and a vertical power device are shown in **Fig. 1**

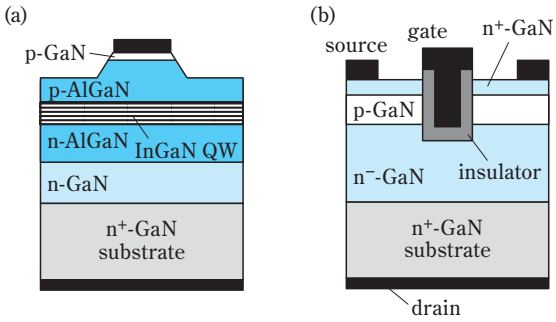


Fig. 1 Devices using free-standing GaN substrates as starting substrates (a) Laser diode and (b) Vertical metal-insulator-semiconductor transistor

In the following we will review the various fabrication methods of GaN single crystal substrates proposed up to now, and discuss their merits and demerits firstly. Then, a review of our original fabrication method of GaN single crystal substrates, the VAS method, will be given together with its recent progress toward improvement in material quality and large wafer fabrication.

Various Manufacturing Methods for GaN Single Crystal Substrates

Here we will describe GaN single crystal substrate fabrication methods proposed by various manufacturers and research organizations up to now from two points of view, “formation method,” focusing on differences in crystal morphology and dislocation reduction mechanism during GaN growth, and “growth method,” focusing on differences in raw materials and crystal deposition mechanisms used in the growth.[15)]

1. Formation Methods for GaN Single Crystal Substrates

Fig. 2 summarizes the formation methods that have been proposed for bulk GaN crystals up to now.[15)] The formation methods are roughly divided into two cases, where self-formed fine crystals or a thin GaN film on a foreign substrate (called a template) are used as seed crystals. Although extremely high quality crystals are obtained through enlargement of self-formed high quality crystal nuclei, it is extremely difficult to expand the crystal size to a practical size. Thus, in most cases at present, the latter template-based method is used for the fabrication of GaN single crystal substrates. The template-based method can be again divided into two

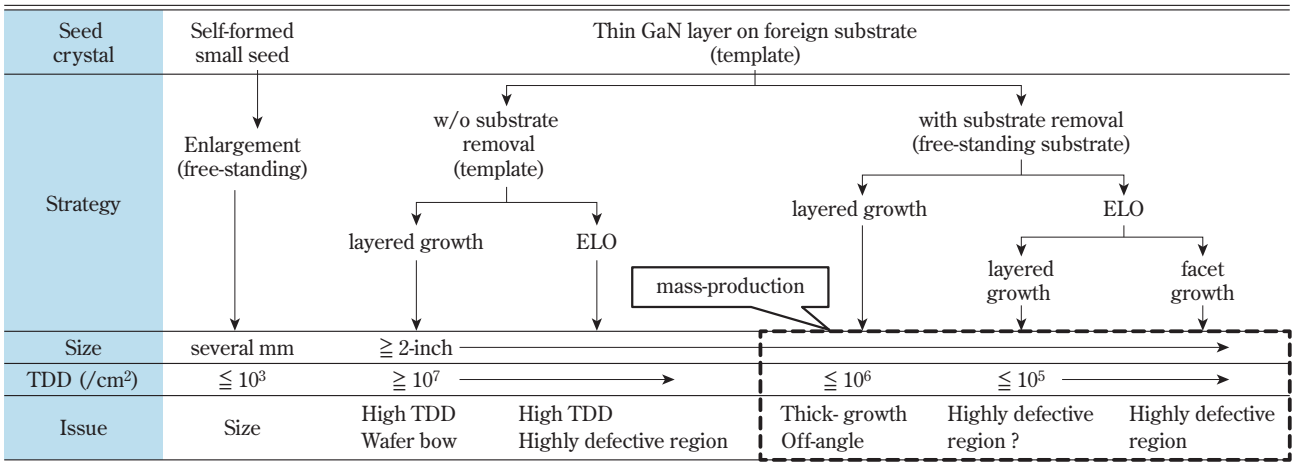


Fig. 2 Summary of strategies for bulk GaN crystal fabrication and their characteristics[15)]

cases, in which the foreign substrate is removed or not removed from the grown crystal. When the foreign substrate is not removed, stress between the foreign substrate and the GaN layer accumulates during the growth as mentioned above. This stress limits the available growth thickness to below about 20 μm, above which risk of crack generation increases. Therefore, it is difficult to achieve low dislocation crystals using this method. On the other hand, if the GaN single crystal is made free-standing by removing the foreign substrate, growth of GaN crystal having a thickness in the millimeter range becomes possible, which enables us to reduce the TDD down to a $10^6/cm^2$ range. All of the GaN single crystal substrates used in the various types of devices at present belong to this final category (foreign substrate and removal). This category is further divided into "layered growth", "ELO + layered growth" and "ELO + facet growth". In "layered growth", the surface is kept flat from an early stage of the crystal growth.[7)–12)] In "ELO + layered growth", so-called epitaxial lateral overgrowth (ELO) is applied at first, where island growth is intentionally introduced in the initial stages of growth by partially covering the base material surface with an insulator mask, on which GaN crystal is difficult to grow. After the ELO-growth, growth conditions are changed so as to make the surface flat.[5)] In the "ELO + facet growth", GaN crystal is grown thickly after ELO-growth, keeping a roughened surface with crystal faces (facets) formed by the ELO-growth.[6)]

Figure 3 shows schematic drawings of the growth process for layered growth and ELO-growth together with processes of dislocation reduction in each method.[15)] A high density dislocation is generated in the initial stages of GaN growth on a foreign substrate, but in layered growth, the TDD reduces gradually through annihilation reactions between dislocations, which move on the surface during the growth in a random-walk fashion. Moreover, with typical GaN crystal growth, a surface parallel to the substrate surface forms a crystal surface known as a +C surface. The +C surface is a chemically stable surface terminated by Ga, and the dislocation generated at the interface with the substrate tends to propagate in a direction perpendicular to the +C surface. Since all of the dislocations are propagated in the same direction (parallel to the +C surface), the dislocation in the layered growth reduces relatively slowly at a rate inversely proportional to the thickness of the GaN layer.[10)–12)] On the other hand, in ELO-growth, the direction of dislocation propagation

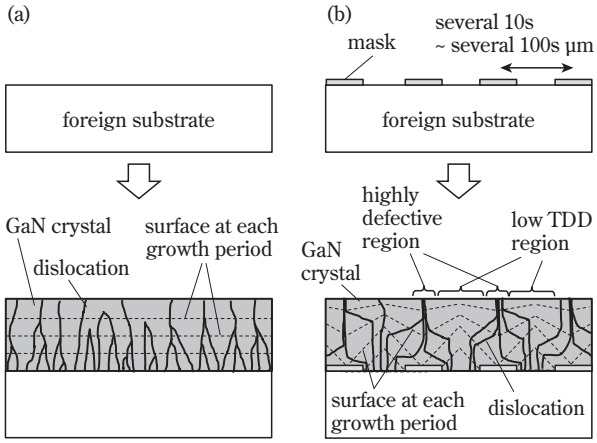


Fig. 3 Main mechanism of dislocation reduction in GaN crystal growth for (a) layered growth and (b) ELO and faceted growth[15)]

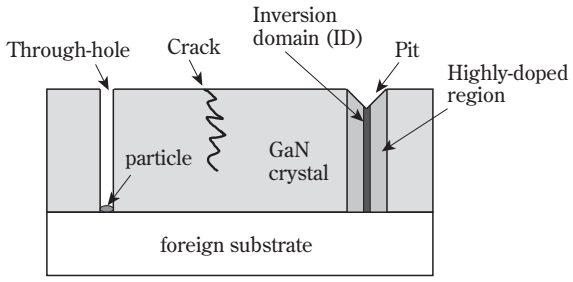


Fig. 4 Various macro-defects observed in GaN crystal

changes when it meets the facet surface, resulting in an increase in the probability of dislocation meeting in comparison with the layered growth. Thus, TDDs in low dislocation areas are reduced more rapidly with ELO than with layered growth. However, in this case, there is the disadvantage of formation of μm to mm size defects (in the following these will be called macro-defects) on the masked areas, such as high TDD areas, through holes, inversion domains (IDs, domains where the surface polarity is reversed to N-terminated (called −C surfaces) instead of usual Ga-terminated) as well as pits and highly-doped regions relating to IDs as shown in **Fig. 4**.[6] These macro-defects tend to deteriorate the performance of devices formed on them.

In layered growth, although these macro-defects are less likely to be generated than in ELO-growth, growth of thick GaN crystal becomes relatively difficult and, hence, reduction of TDDs as well as off-angle distribution also become difficult as explained below. **Fig. 5** shows an example of a GaN substrate fabrication method using layered growth on a foreign substrate. Here, a method is shown in which the main GaN crystal is grown on seed crystal having many voids and is removed from the foreign substrate at the voided region. If the voids in the seed crystal are small, fine GaN crystal nuclei with sizes in the micron range or less are formed in the initial stages of growth as shown in **Fig. 5** (the nuclei being drawn large so they are easy to see in this drawing). When these GaN crystal nuclei coalesce, bowing occurs in the C-plane, which causes a distribution of crystal orientation (deviation from C-plane, called the "off angle") in the wafer surface fabricated by polishing the GaN crystal. Presence of such off-angle distribution of the substrate is a cause of variation in the characteristics of the devices formed on the wafer[16), 17)] since incorporation efficiency of impurities and alloy composition are often dependent on off-angle. Therefore it is

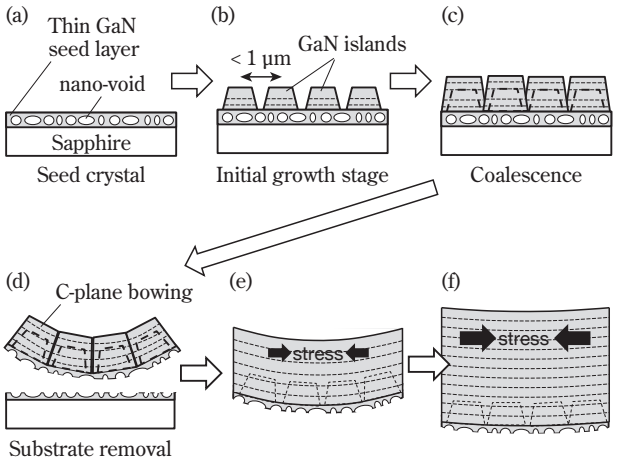


Fig. 5 An example of GaN bulk crystal fabrication sequence by thick layer growth on seed crystal with nano-voids

preferable to have a small off-angle distribution. If the GaN crystal is made thicker after flattening, curvature of the C-plane is reduced as shown in **Fig. 5** (e) (f), but the risk of crack formation increases (see **Fig. 4**), in turn, due to increase in accumulated stress inside the crystal against the initial C plane bowing.

In ELO-growth, on the other hand, the C-plane bowing as well as the related stress accumulation are relaxed largely because of the presence of macro-defects. Therefore, the GaN layer can be grown thicker than in the case of layered growth. The availability of thicker layer growth as well as the rapid dislocation reduction mechanism of the ELO-method make it easy to reduce TDD down to the $10^5/cm^2$ range. However, care must be taken when applying this substrate to actual devices since removal of macro-defects by additional growth is difficult and application of a polishing process to the crystal surface cannot remove the macro-defects inside the bulk even if a flat surface is realized by the polishing.

2. Growth Methods for GaN Single Crystal Substrates

Next, the "growth methods" for GaN crystals will be explained. Typical methods are vapor phase methods including metal-organic vapor phrase epitaxy (MOVPE) and hydride vapor phase epitaxy (HVPE), and solution methods (note that they are different from "melt"-growth for GaAs and InP) such as the ammonothermal and the Na-flux methods. The features of these growth methods are given in **Table 1**.

Table 1 Method of GaN crystal growth and their characteristics

	Growth method	Features	Present status
Vapor phase	Metal-organic vapor phase epitaxy (MOVPE)	GaN is grown by reaction between Trimethylgallium and NH_3.	Used for ELO-template growth in R&D stage of LDs.
	Hydride vapor phase epitaxy (HVPE)	GaN is grown by reaction between GaCl and NH_3.	Main method for mass-production of GaN substrates
Liquid phase	Ammonothermal method	GaN is re-crystallized from GaN raw material dissolved in supercritical NH_3.	R&D phase.
	Na-flux method	GaN is grown by reaction between Ga and N_2 both dissolved in Na-melt.	R&D phase.

In the early stages of LD development, MOVPE was widely used to perform GaN crystal growth without substrate removal shown in **Fig. 2**.[4] However, at present, it is not used for the growth of single-crystal, free-standing GaN substrates, in which growth of GaN crystal having thickness in millimeter range is required, because of its relatively slow growth rate of around several μm/h. Instead of this, the MOVPE method has been the main epitaxial growth tool of GaN-based thin layers because of its high thickness controllability. Most of the GaN single crystal substrates under mass-production are grown by HVPE at present.[6)–12), 18), 19)] This is due to its extremely high growth rate of over 100 μm/h and relatively high material purity, as well as an availability of good growth condition control enabling growth mode changes between the ELO and layered growth required for GaN single-crystal substrate growth. The disadvantage of the HVPE-method is a limitation in the amount of GaN crystals available within a single HVPE growth run because of chlorides deposit in the exhaust system.

On the other hand, in liquid phase methods such as the ammonothermal and Na-flux methods,[20), 21)] there are no limits caused by the exhaust as in the case of HVPE growth since GaN crystals are grown in a closed solution system. Hence, long crystals can be achieved by extremely long growth period over several days to several months. Until now, achievement of several-mm thick GaN crystals having extremely low TDD through natural ELO-like growth is reported for these methods. However, issues on low material purity due to incorporation of impurities from the autoclave wall as well as the difficulty in precise growth condition control needed to suppress the macro-defect formation remain to be solved. Therefore, the liquid phase growth methods have still remained in the development stage.

Fabrication of GaN Single Crystal Substrates by Void Assisted Separation (VAS)

1. Overview of VAS

The formation sequence of the VAS-method for fabrication of GaN single crystal substrates developed by us is basically the same as that shown in **Fig. 5**. Thick GaN crystal is grown on a template with internal voids on a foreign substrate, and a free-standing GaN single crystal substrate is achieved by separating the GaN crystal from the substrate.[7] In the VAS-method, the HVPE method giving high growth rate as mentioned previously is used. **Fig. 6** shows a schematic diagram of the HVPE growth equipment. GaCl gas is generated by supplying HCl gas to a Ga melt placed at an up-stream high temperature region within the equipment, and NH_3 gas is supplied from another line. These gases react on the substrate placed at the down-stream region which is kept at around 1100°C, leading to the growth of the GaN crystal. The voided seed substrate is made by annealing a MOVPE-grown template, i.e. a GaN thin layer on a sapphire substrate, covered by Ti thin film as is shown in **Fig. 7** (a). During the annealing process, the Ti thin film changes into a net-like structure of TiN, and innumerable nanometer sized voids are also formed within the GaN

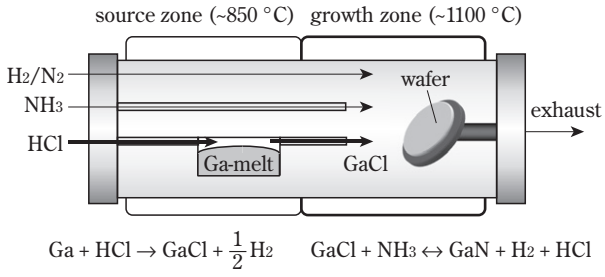


Fig. 6 Schematic drawing of HVPE equipment

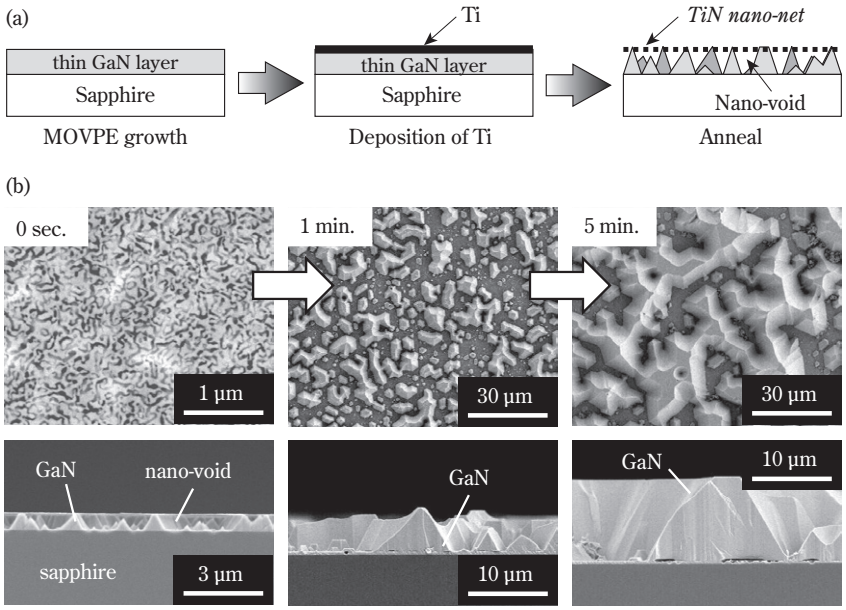


Fig. 7 (a) Sequence of seed crystal formation in void-assisted separation method (VAS) and (b) SEM photograph of initial stage of GaN substrate growth by HVPE on the voided-seed crystal

layer (left side of figure in **Fig. 7** (b)). When GaN crystal is grown on these voids by HVPE, the small GaN nuclei are formed at first on the TiN net-like structure as shown in **Fig. 7** (b) and **Fig. 5**. Further growth induces coalescence of the initial GaN nuclei, leading to formation of a continuous GaN layer. As can be seen on the right-hand side of the figure in **Fig. 7** (b), voids remain between the seed crystal and the HVPE growth layer even after the main GaN crystal growth. Therefore, the GaN growth in the VAS-method proceeds keeping the stress between the GaN crystal and the sapphire substrate far smaller than that for the GaN crystal growth without substrate removal. Hence, growth of GaN crystal having a thickness in the millimeter range becomes possible with the VAS method although the available GaN thickness in the growth without substrate removal is limited at most to 100 μm. During the growth of such a thick GaN crystal, the TDD is reduced down to the lower half of the $10^6/cm^2$ range because of the TDD reduction through annihilation reactions between dislocations randomly moving on the growth front as mentioned previously. Since nanometer size voids are used in the VAS-method instead of a several to several hundred micron size pattern used in the ELO-based method, GaN single-crystal substrates having a uniformly low dislocation density across the entire substrate surface as shown in **Fig. 8** can be achieved by the VAS-method.

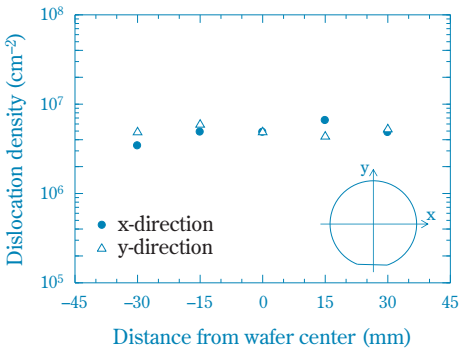


Fig. 8 Threading dislocation density (TDD) distribution of free-standing GaN substrate made by the VAS-method

2. Suppression of Macro Defects in GaN Single Crystal Substrates by VAS

As described previously, macro-defects as shown in **Fig. 4** are likely to occur during GaN crystal growth. They are a serious issue with the ELO method, but they have also been an important problem even in the VAS-method particularly at the beginning of its development stage. Since these macro-defects occur because of the nature of the GaN crystal itself, reports on their origin and suppression method have been often provided from other research institutions for free-standing GaN substrates made neither by the VAS-method nor HVPE-method.[22), 23)]

Fig. 9 (a) shows a photograph of an as-grown GaN

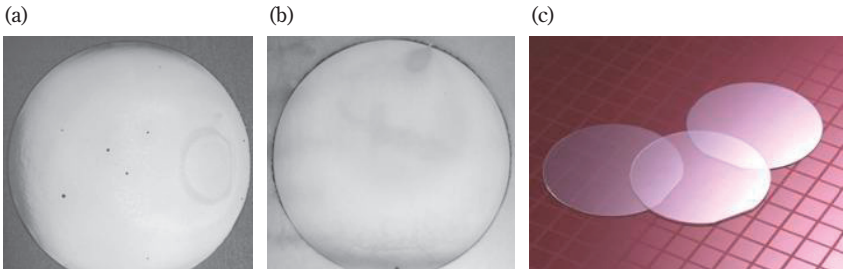


Fig. 9 Photographs of free-standing GaN substrates made by the VAS method. (a) and (b) as-grown GaN bulk crystals before and after growth optimization, respectively. (c) Free-standing GaN wafers after application of polishing process.

crystal for 2-inch free-standing substrate made at the initial stage of our development. The black dots seen in this figure are pits and through holes caused by IDs. On the other hand, the gray elliptical shape pattern on the right side is residual metallic Ga caused by evaporation of the back surface crystal during growth, and it can be eliminated by back surface polishing. In the initial development stage of the VAS-method, it was difficult to find growth conditions satisfying all of substrate removal, TDD reduction and suppression of these macro-defects. However, this difficulty was overcome through the development of our original HVPE growth equipment allowing much more precise growth condition control than with conventional HVPE equipment, by which suppression of all of the above mentioned macro-defects within the entire wafer surface became possible. **Fig. 9** (b) is a photograph of an as-grown free-standing GaN substrate after the improvements. No black dots corresponding to the pits and through holes seen in **Fig. 9** (a) were observed. Additionally, absence of any ID on the wafer surface was also confirmed by an optical microscope inspection as well as by growth tests using MOVPE. **Fig. 9** (c) shows a photograph of 2-inch GaN single crystal substrates fabricated by applying a polishing process to such macro-defect-free GaN crystals. They are transparent without coloration and deformation in transmission images, indicating the realization of high quality GaN single crystal substrates which are free from high-density impurities and defects.

3. Further Reductions of Dislocations in GaN Single Crystal Substrates

At the beginning of development, the dislocation density of GaN single crystal substrates made by the VAS-method was in the lower half of the $10^6/cm^2$ range, which was sufficiently low enough for blue LDs and high-power LEDs, and, hence, our GaN substrate is widely used in these applications. However, further reduction of TDD might be necessary for future extremely high-power LDs and LEDs as well as for next-generation highly-efficient power devices. In this section, we will introduce our recent efforts and achievements toward applications to such next generation devices.

The dislocation reducing mechanism in the VAS-method corresponds to that for GaN single crystal substrates fabricated by "layered growth" as described previously, in which dislocations are reduced through annihilation reactions between dislocations moving on the surface in a random-walk fashion during the growth. In this mechanism, the TDD is expected to be inversely proportional to the GaN growth thickness. However, when the growth conditions for the initial development stage are used, reduction in TDD stopped at certain critical thicknesses as shown in A or B in **Fig. 10** (a) although they reduced in an inverse proportion to growth thickness when the thickness was smaller than the critical value.[10] This TDD behavior can be explained in terms of plastic deformation of crystal through generation of new dislocations. With the increase in the growth thickness, various stresses such as that due to initial C-plane bowing as shown in **Fig. 5** and that due to adhesion between the GaN crystal and growth parts by parasitic deposition tend to increase. When the thickness becomes larger than the critical value, these stresses generate new dislocations inside the GaN crystal and lead plastic deformation of the crystal. When the crystal thickness is far beyond the critical thickness, breakage and cracks in the crystal occur, and it is difficult to obtain GaN crystals having a sufficient size for products. Because of this phenomenon, the thickness of GaN crystal that could be grown by VAS-method was approximately 1 mm in the initial

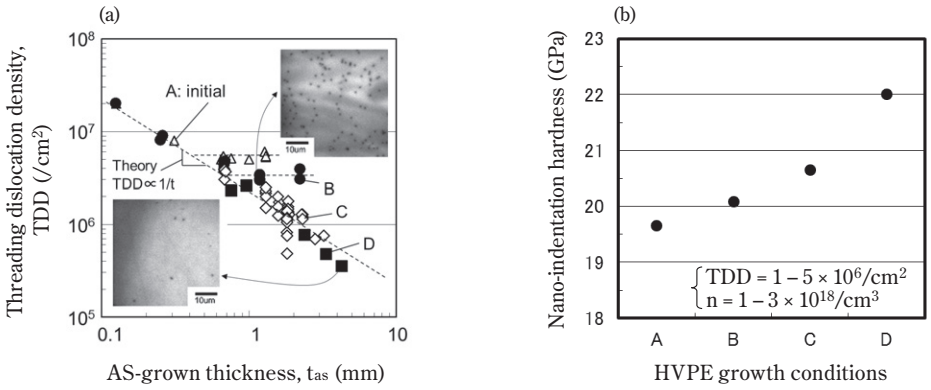


Fig. 10 Effect of GaN crystal hardness on the available as-grown thickness, t_{as} and TDDs. (a) Relationships between t_{as} and TDD for the macro-defect-free GaN substrates grown by the VAS-method using the conditions A-D. Cathodoluminescence images for GaN substrates grown using the conditions B and D are shown as insets. (b) Dependence of nano-indentation hardness values of the GaN crystal grown by the VAS-method on HVPE-growth conditions A-D.

stages of development, and the dislocation density for the GaN single crystal substrates was limited to the lower half of the $10^6/cm^2$ range.

The above TDD saturating phenomenon occurs if the GaN single crystal substrate does not include macro-defects as shown in preceding paragraph. When a large number of macro-defects such as IDs were intentionally introduced into the GaN single crystal substrate, it was possible to grow 2–3 mm thick GaN crystals without cracks even with the same growth conditions as initial stage of the development. In this case, the TDDs of the surface area free-from ID could be reduced to $1 \times 10^6/cm^2$ or less. However, IDs are defects running across the whole bulk crystal thickness, and they cannot be removed by polishing processes. When device structures are grown on IDs, the device performance might deteriorate since the growth rate and incorporation of impurities for IDs are different from normal regions Therefore, the GaN single crystal substrates fabricated using this kind of GaN crystal cannot be used for practical devices.

We have successfully overcome such a trade-off between the crystal thickness and introduction of macro-defects by introducing control of GaN crystal hardness through precise HVPE growth condition control. By making the GaN crystal harder, growth of much thicker GaN crystals than before becomes possible without introducing macro defects. **Fig. 10** (b) summarizes the hardness values measured by the nano-indentations for the GaN crystals grown under various growth conditions. Although the hardness of the GaN crystal was only 19.6 GPa under the initial condition A, it increased with the growth condition improvement from B to D. The hardness value was increased to 22 GPa with conditions D.[12] Although there exist several reports on nano-indentation measurements for GaN single crystal substrates from other research groups, nobody has reported the possibility of crystal hardness control by the growth conditions. Moreover, the present hardness value obtained by the conditions D is the maximum value reported up to now.[24)–28)]

Along with the increases in hardness, the available thickness of the macro-defect-free GaN crystals without introducing cracks increased as shown in **Fig. 10** (a). Under the conditions D, a maximum crystal thickness of 6 mm as is shown in **Fig. 11** was obtained, where the TDD on the top surface was reduced to the lower half of the $10^5/cm^2$ range. Moreover, no saturation trend

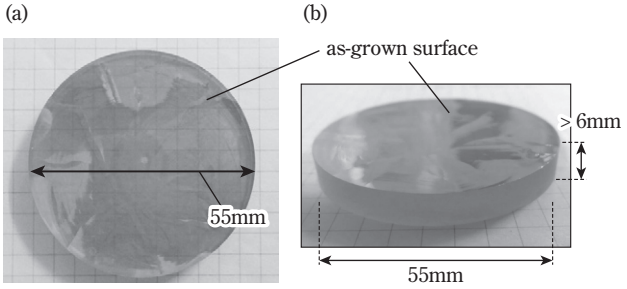


Fig. 11 Photographs of thick GaN bulk crystal for 2-inch wafer grown using the conditions D after cylindrical grinding. (a) Top-view and (b) bird's-eye view.

was seen for the TDD even at the maximum crystal thickness for the conditions D as seen in **Fig. 10** (a), implying the possibility of realization of much thicker GaN crystals. At present, the available GaN crystal thickness at SCIOCS Co., Ltd. is limited by the configuration of the HVPE system rather than cracking of GaN crystals. Thus, we can expect further increase in the GaN growth thickness and reduction in TDD in the future by further improving the structure of the HVPE equipment.

Usually, plastic deformation of metals including a large number of dislocations is explained by the movement of existing dislocations, but it is impossible to use this concept to explain the present results of nano-indentation measurements for free-standing GaN substrates. The TDD of the GaN single crystal substrates was in the $10^6/cm^2$ range, which corresponds to a distance between neighboring dislocations of around 10 μm. Since nano-indentation measurements were carried out using an indenter with a tip diameter of several tens of nanometers with its indentation depth about 100 nm, the possibility of the tip of the indenter directly hitting at a dislocation is not high. Therefore, the possibility that the movement of dislocations existing before indentation would affect the results of the measurements is expected to be low. Instead of this, the present crystal hardness can be considered as a resistance against the plastic deformation of a dislocation-free crystal through the generation of new dislocations. The origin of the differences in difficulty of dislocation generation for the similar GaN crystal are not clear at present. One possible explanation is the difference in vacancy concentration in each GaN crystal, which can cause differences in the difficulty of introduction of dislocation loops through aggregation of vacancies.

If this hypothesis is correct, we can assume that GaN crystals grown under conditions D have a lower vacancy concentration within the crystal than those grown under conventional conditions A to C; therefore, the generation of new dislocations is suppressed in thick crystal growth under the conditions D, which led to further reduction in TDDs. The behavior of vacancies within the GaN crystal has not been clarified yet. However, several first-principal calculations showed the presence of stable clusters formed from 10 or more vacancies in GaAs crystals[29] and the formation of stable dislocation loops in metallic Al through aggregation of vacancies.[30] We hope for future progress in similar research on vacancy behavior in GaN crystals.

4. Increase in sizes of GaN Single Crystal Substrates

Increasing the diameter of substrates is an important issue for reducing the costs of GaN devices. Although the size of commercially-available GaN single crystal substrates at present is mostly 2-inch, it is necessary to expand this to 4-inch or 6-inch diameters in the future. With VAS, it is relatively easy to fabricate large GaN single crystal substrates, if a large-size seed sapphire wafer can be prepared. However, simple application of crystal growth similar to that for small-diameter wafers will not give substrates that can be used for practical device fabrication. This is due to difficulty in achievement of an off-angle variation similar to that of small-diameter wafers in large-diameter wafers. As described previously, the characteristics of devices fabricated on a substrate are affected by the off angle, and, hence, large off-angle variation tends to reduce the device yield. Thus, the off-angle variation must be held to a level that is the same as for small-diameter substrates or lower, even if the substrate has a large diameter. However, since the GaN crystal is grown with C-plane bowing as shown in **Fig. 5**, large GaN wafers inevitably have larger off-angle variation than small wafers if both are made from similar crystal having the same C-plane bowing as shown in **Fig. 12**. In this case, the off-angle variation of the large wafer will exceed the acceptable range for fabrication of practical devices. For example, when the thickness of the GaN growth layer is 1 mm, the off-angle variation for a 2-inch wafer is approximately 0.3–0.4° (measured at positions ±15 mm from the substrate center). However, in the case of fabricating a 4-inch wafer with a crystal of similar thickness, the off

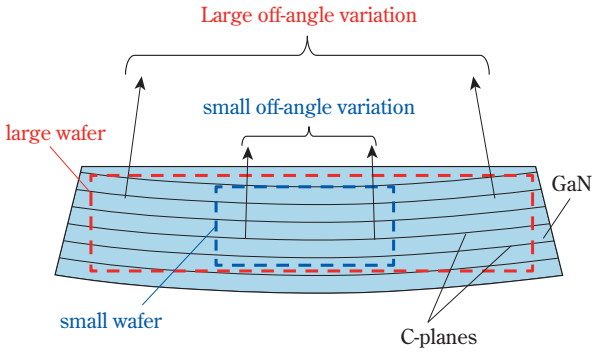
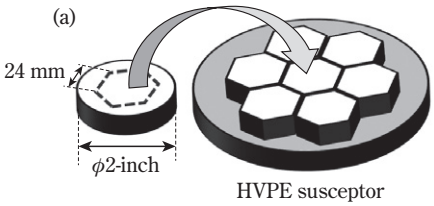


Fig. 12 Schematic explanation of difficulty in achieving small off-angle variation for large size wafer in comparison with small wafer. If C-plane curvature of GaN crystals are the same, large wafer should have larger off-angle variation than small wafer.

angle distribution increases twofold to 0.6–0.8° (measured at positions ±30 mm from the substrate center).

At SCIOCS Co., Ltd., two different approaches have been tried for reducing off-angle variation in large-diameter substrates. One is called the tiling method, in which a large diameter substrate is realized by bonding hexagonal tiles of GaN crystal which were made by cutting 2-inch substrates, through HVPE overgrowth of GaN crystal as shown in **Fig. 13** (a). Using this method, we were successful in achieving the world's largest GaN substrate with a 7-inch diameter as shown in **Fig. 13** (b).[31] By using this method, it is possible to achieve a large-diameter substrate having an off-angle variation equal to a standard 2-inch substrate if the off-angles themselves and their variation for each tile are properly adjusted. Although tiling substrates include a crystal lattice disorder at the bonded parts of adjacent tiles, we have confirmed that slicing and polishing processes as well as HVPE-regrowth of thick GaN layer can be applied to such tiling substrates similar to normal GaN crystals.



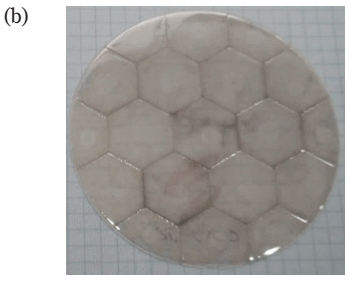


Fig. 13 (a) Concept of tiling method and (b) Photograph of 7-inch freestanding GaN substrate made by the tiling method

The other approach is a reduction in the off-angle variation of a GaN single crystal substrate by increasing the growth thickness of the GaN crystal as shown in **Fig. 5**. Also in this case, increasing GaN crystal thickness based on the hardness control mentioned above was very effective. Based on this, we have succeeded in fabricating 2–6 inch GaN single crystal substrates with small off-angle variations. Photographs of the 4-inch and 6-inch diameter GaN single crystal substrates fabricated by this method are shown in **Fig. 14** together with a conventional 2-inch diameter substrate. The 2-inch and 4-inch substrates have been polished (rough surface finishing on the back surface), and transparent crystals with no coloration have been achieved. The 6-inch substrate is an as-grown crystal that has not been polished. Therefore, it showed metallic color due to metallic Ga residue which was formed on the back surface during growth. However, it basically has the same crystal quality as the 2-inch and 4-inch substrates. As a result of increasing the thickness of the GaN layer, macro-defect-free GaN single crystal substrates having low dislocation densities in the $10^5/cm^2$ range and small off angle variations (maximum value–minimum value, 0.1° for the 2-inch substrate and 0.2° for the 4-inch substrate) were realized.

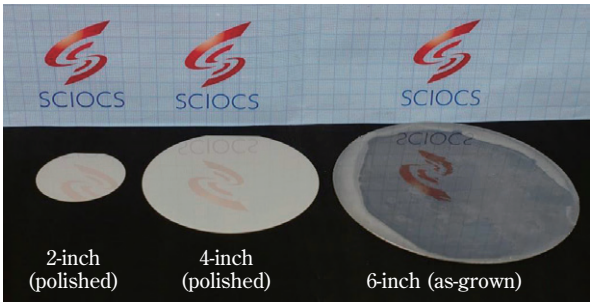


Fig. 14 Photograph of 2, 4 and 6-inch size macro-defect-free GaN wafers grown using the conditions D. The 2 and 4-inch wafers were single side polished wafers. On the other hand, the 6-inch one was the as-grown wafer with residual Ga on its backside.

Summary

Review of various fabrication technologies for GaN single-crystal wafers reported to date as well as detailed description of our VAS-method for GaN single crystal fabrication were given in this paper.

Using the VAS-method, we have realized the GaN single crystal substrates having uniform and low TDD (in the lower half of the $10^6/cm^2$ range) and free from macro-defects, which deteriorate device operations made on them, for the first time. Additionally, we also showed the availability of GaN crystal hardness control thorough HVPE-condition adjustment for the first time.

Based on this, GaN single crystal substrates having extremely low TDD in the lower half of the $10^5/cm^2$ range, as well as those having large diameters of up to 6 inches were realized. The world largest GaN single crystal substrate with a 7-inch diameter was also realized using the tiling method.

We hope that GaN single crystal substrates produced by the VAS-method can make important contributions to the expansion of application areas for blue LDs and high-efficiency LEDs including general illumination, automotive headlights and so on. We also hope they can contribute to the realization and commercialization of next-generation environmental devices including GaN-based power devices.

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